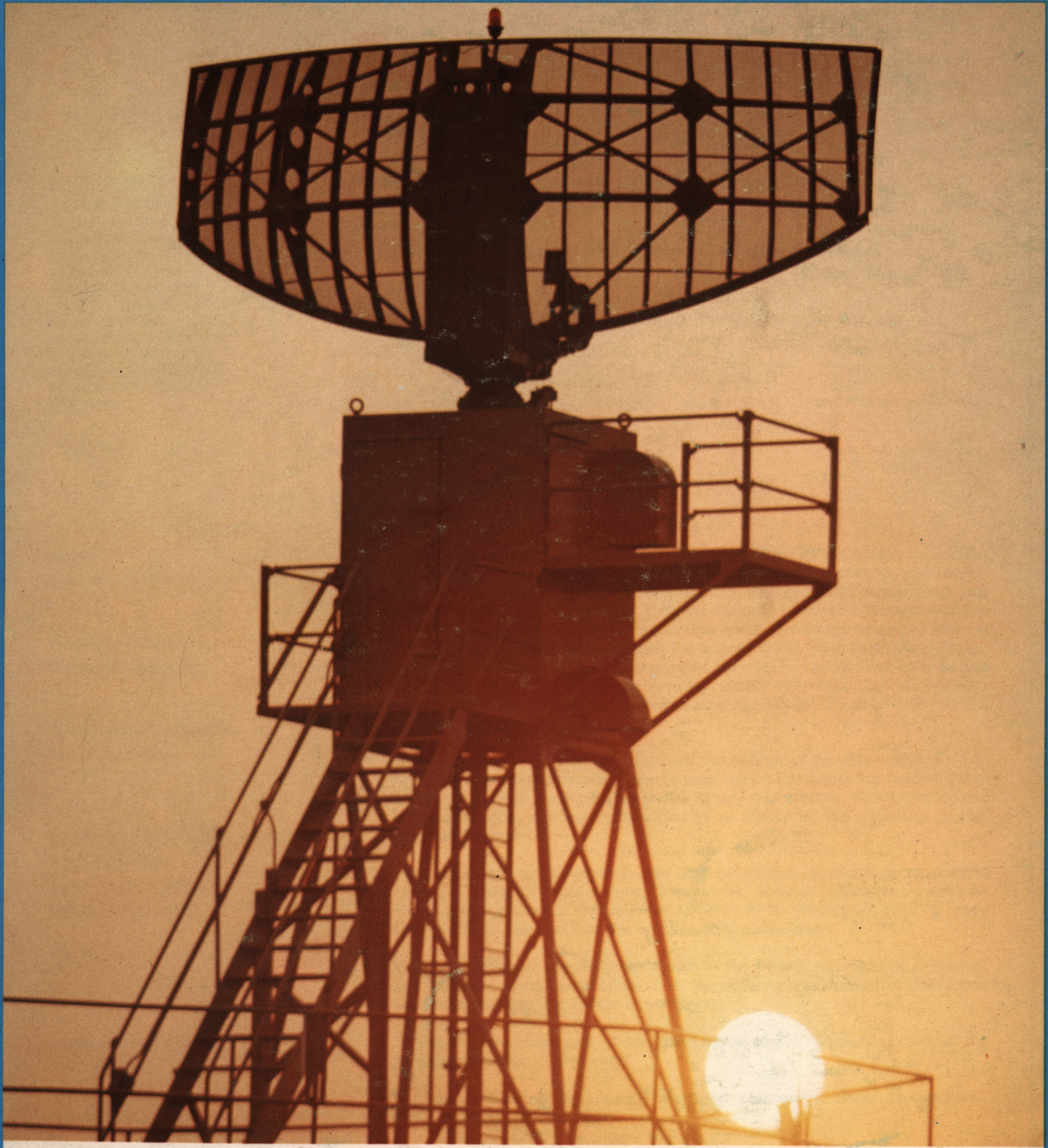
N. G. W.

Mullard

Technical Communications

Volume 14 Number 137

January 1978



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Mullard Technical Communications
ISSN 0027—3139

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Cover picture:

Secondary surveillance radar at London Airport, Heathrow (photo courtesy British Airports). Mullard manufactures a wide range of components for all microwave applications. Included in this issue is an article describing the behaviour of microwave crystal detectors.

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New Road, Mitcham,
Surrey, CR4 4XY

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Made and Printed in England by
The Yale Press Ltd.,
Carmichael Road, London, S.E.25.
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An SMPS without mains isolation for tv receivers

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The third in a series of four articles about television switched-mode power supplies, this article describes a forward converter circuit without mains isolation. General principles of operation and design considerations are given. A practical circuit for 220V mains is described together with suggested board layout, and with performance details.

INTRODUCTION

In the earlier articles in this series (Refs.1 and 2) it was shown that, if mains isolation is not required, the simplest and most cost-effective type of switched-mode power supply for a television receiver is one that uses a forward converter. It was also shown that it is advantageous to derive the drive for the horizontal deflection output transistor from the SMPS and to switch the horizontal deflection and SMPS output transistors in the non-simultaneous mode. Such a circuit is discussed in this article; the same design rules are also valid for SMPS circuits that do not use base drive.

Principles of operation

A simplified circuit diagram of a forward converter, together with waveforms and definitions, is given in Fig.1.

When the transistor conducts, energy is stored in the choke. The voltage across the choke and the rate of change of current flowing through the choke are related by the equation:

$$V_L = -L\frac{di_L}{dt}, \qquad \ldots(1)$$

which can be rewritten:

$$\Delta I_{L(\delta T)} = \frac{V_i - V_o}{L}\delta T. \qquad \ldots(2)$$

When the transistor ceases to conduct, the polarity of the voltage across the choke reverses, and the stored energy is passed to the load via the flywheel diode. During this period (T − δT), the decrease of the current through the choke is:

$$\Delta I_{L(T-\delta T)} = \frac{V_o T}{L}(1-\delta). \qquad \ldots(3)$$

Equilibrium is reached when the increase of choke current during the transistor conduction period is equal to the decrease of choke current during the period when the transistor is cut-off. This condition occurs when:

$$\frac{V_i - V_o}{L}\delta T = \frac{V_o T}{L}(1-\delta).$$

Solving this equation for V_o gives:

$$V_o = \delta V_i. \qquad \ldots(4)$$

The output voltage from this type of converter can therefore be stabilised against input voltage (rectified mains) variations by controlling the duty factor δ of the drive pulses applied to the base of the SMPS output transistor.

The capacitor connected across the load in Fig.1 is a smoothing capacitor and smooths the choke current I_L to produce an output voltage V_o which is almost ripple-free.

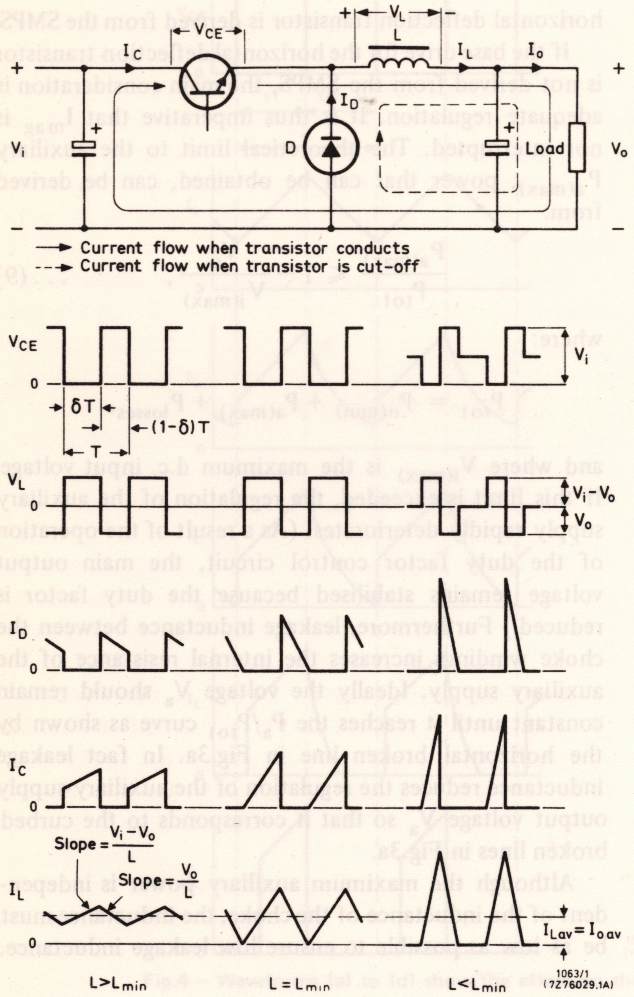
Minimum choke inductance

The current I_L has a sawtooth ripple component which is inversely proportional to the inductance L of the choke. This is illustrated by the three waveforms for I_L shown in Fig.1. The minimum value of inductance for the choke is that which will limit the peak-to-peak value of the ripple current to twice the average value of the minimum load current as shown in the centre waveform for I_L in Fig.1. This can be expressed as:

$$\frac{V_o T}{L}(1-\delta) = 2I_{o(av)}. \qquad \ldots(5)$$

Substituting V_o/V_i for δ and P_o/V_o for $I_{o(av)}$, and then solving the equation for L gives:

$$L_{min} = \frac{V_o{}^2 T}{2P_o}\left(1 - \frac{V_o}{V_i}\right). \qquad \ldots(6)$$



$$V_o = \delta V_i$$

$$L_{min} = \frac{V_o{}^2 T}{2P_o}\left(1 - \frac{V_o}{V_i}\right)$$

$$I_{C(pk)} = \frac{V_o T}{2L}\left(1 - \frac{V_o}{V_i}\right) + \frac{P_o}{V_o}$$

$$V_{CE(pk)} = V_i$$

Fig.1 – Basic circuit of a forward d.c.-to-d.c. converter with waveforms showing the effect of variation of the inductance of the choke

If the choke inductance is greater than this minimum value, then the amplitude of the sawtooth ripple current is decreased (see the left-hand waveform for I_L in Fig.1). If the choke inductance is smaller than the minimum value, the amplitude of the sawtooth will be greater than twice the average load current and the choke current will be interrupted as shown by the right-hand waveforms in Fig.1. This results in:

1) increased internal impedance of the supply and thus poor regulation;
2) increased peak currents through the transistor and the flywheel diode;
3) a choke voltage waveform shape that is unsuitable for driving the horizontal deflection output transistor.

Peak collector current of output transistor

The peak collector current passed by the SMPS output transistor is given by:

$$\begin{aligned} I_{C(pk)} &= I_{L(pk)}, \\ &= \frac{I_{ripple}}{2} + I_{o(av)}, \\ &= \frac{V_o T(1-\delta)}{2L} + I_{o(av)}. \qquad \ldots(7) \end{aligned}$$

Substituting V_o/V_i for δ and P_o/V_o for $I_{o(av)}$ gives:

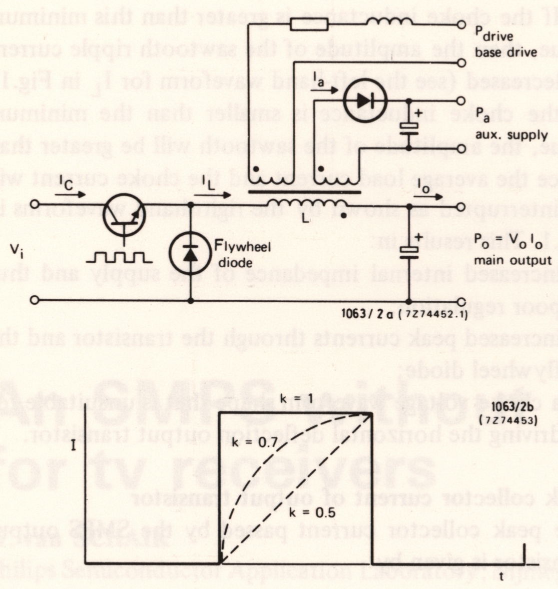
$$I_{C(pk)} = \frac{V_o T}{2L}\left(1 - \frac{V_o}{V_i}\right) + \frac{P_o}{V_o}. \qquad \ldots(8)$$

Deriving auxiliary power from the SMPS

Since the voltage across the choke is stabilised during the period when the SMPS output transistor is not conducting, auxiliary stabilised low voltages can be obtained by adding a secondary winding to the choke. These voltages are then rectified by a diode that conducts during the flywheel period. Such a circuit is shown in Fig.2 together with associated definitions.

In the description of the basic d.c.-to-d.c. forward converter, the choke core was considered as magnetised only by the current I_L flowing through the choke. As it is essential that the choke core should always be magnetised, this current must not be interrupted. When one or two secondary windings are wound on to the choke, the currents flowing in these windings contribute to the magnetisation of the choke core. (It is assumed that the total load on an SMPS in a tv receiver is kept constant.) The choke primary current may, in this case, be interrupted providing that there is sufficient current flowing in the secondary windings to maintain the magnetic field in the choke core.

The load on the auxiliary supply decreases the amount of energy recovered by the flywheel diode. To illustrate



$$P_{tot} = P_o + P_a + P_{drive} + P_{loss}$$

$$L_{min} = \frac{V_o{}^2 T}{2P_{tot(min)}}\left(1 - \frac{V_o}{V_{i(max)}}\right)$$

$$I_{C(pk)} = \frac{V_o T}{2L}\left(1 - \frac{V_o}{V_{i(min)}}\right) + \frac{P_{tot(max)}}{V_o}$$

$$V_{CE(pk)} = V_{i(max)}$$

$$\frac{P_{a(max)}}{P_{tot}} \leqslant 1 - \frac{V_o}{V_{i(max)}}\ *$$

$$\frac{P_{a(max)} + P_{drive}}{P_{tot}} \leqslant k\left(1 - \frac{L_{min}}{L}\right)\left(1 - \frac{V_o}{V_{i(max)}}\right)\ \dagger$$

* Without base drive

† With base drive

Fig.2 – (a) Deriving auxiliary power from the SMPS;
(b) the current form factor k of $P_a + P_{drive}$

this in Fig.3b we have the concept of a notional magnetising current I_{mag}, which is the sum of the choke primary current I_L and the transformed secondary currents. The sawtooth outline of the I_L waveform in Fig.1 is maintained and the choke core magnetisation remains the same but, during the flywheel period, the current through the flywheel diode is greatly diminished and is interrupted for part of the period. The difference in ampere-turns is made up by the currents in the secondary windings.

The amount of auxiliary power that can be derived from the SMPS is limited. The actual amount of auxiliary power available depends on whether base drive for the horizontal deflection transistor is derived from the SMPS.

If the base drive for the horizontal deflection transistor is not derived from the SMPS, the main consideration is adequate regulation. It is thus imperative that I_{mag} is not interrupted. The theoretical limit to the auxiliary $P_{a(max)}$, power that can be obtained, can be derived from:

$$\frac{P_{a(max)}}{P_{tot}} \leqslant 1 - \frac{V_o}{V_{i(max)}}, \qquad \ldots (9)$$

where:

$$P_{tot} = P_{o(min)} + P_{a(max)} + P_{losses},$$

and where $V_{i(max)}$ is the maximum d.c. input voltage. If this limit is exceeded, the regulation of the auxiliary supply rapidly deteriorates. (As a result of the operation of the duty factor control circuit, the main output voltage remains stabilised because the duty factor is reduced.) Furthermore, leakage inductance between the choke windings increases the internal resistance of the auxiliary supply. Ideally the voltage V_a should remain constant until it reaches the P_a/P_{tot} curve as shown by the horizontal broken line in Fig.3a. In fact leakage inductance reduces the regulation of the auxiliary-supply output voltage V_a so that it corresponds to the curbed broken lines in Fig.3a.

Although the maximum auxiliary power is independent of the inductance of the choke, the inductance must be as low as possible to ensure low leakage inductance.

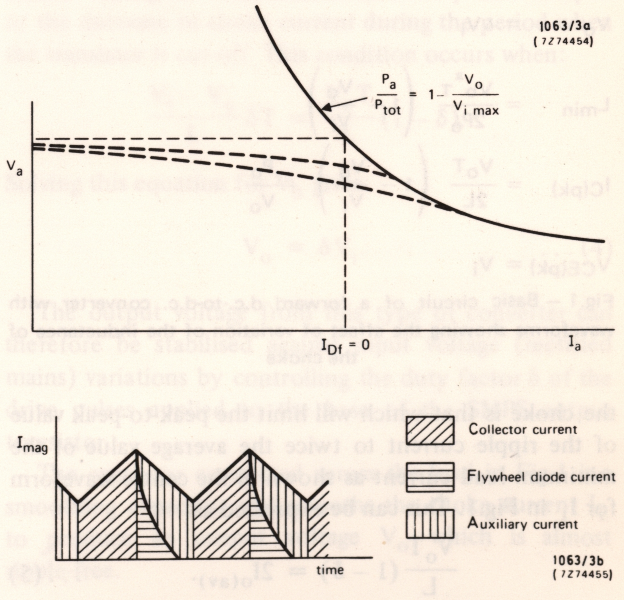


Fig.3 – Limitation of auxiliary power when horizontal deflection drive is not required from the SMPS

(a) Regulation of auxiliary supply. The broken lines show the effect of increasing leakage inductance

(b) Distribution of choke magnetising current between the transistor, the flywheel diode and the auxiliary supply diode

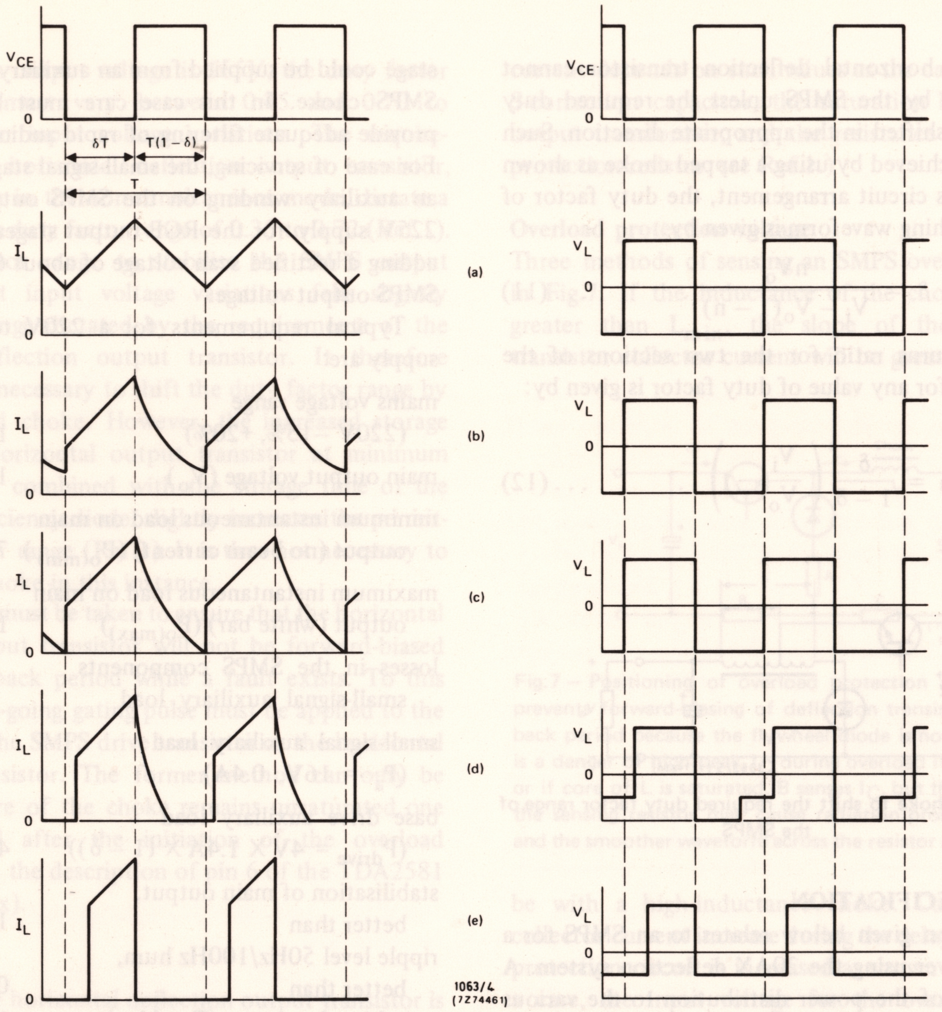


Fig.4 – Waveforms (a) to (d) show the effect on the choke primary voltage and current of keeping P_{tot} constant whilst increasing auxiliary power. Waveforms (e) represent the theoretical limit for auxiliary power if horizontal drive is not required (flywheel diode no longer conducts). Only waveforms (a) to (c) are acceptable if horizontal drive is required. Subsequent choke voltage waveforms exhibit distortion and duty factor variation

This conflicts with the requirement for a high choke inductance (uninterrupted choke current) already discussed. Certain other factors that influence the choice of choke inductance are discussed later.

If auxiliary power or base drive (or both) for the horizontal deflection transistor should be derived from the SMPS, it becomes essential that the inductance of the choke is greater than L_{min} if the correct base drive waveform and duty factor are to be maintained. For the same reason the available auxiliary power is reduced to the value that ensures that the flywheel diode conduction period is never less than $(T - \delta T)$. The maximum available auxiliary power can be derived from:

$$\frac{P_{a(max)} + P_{drive}}{P_{tot}} \leqslant k\left(1 - \frac{L_{min}}{L}\right)\left(1 - \frac{V_o}{V_{i(max)}}\right), \qquad \ldots (10)$$

where:

$$P_{tot} = P_{o(min)} + P_{a(max)} + P_{drive} + P_{losses},$$

and k is the form factor of the auxiliary currents as shown in Fig.2b. However, if L is much greater than L_{min}, then $V_{i(min)}$ must be substituted for $V_{i(max)}$.

Main and auxiliary load transients must be smoothed to prevent them causing overshoots in duty factor which result in variations in transistor storage time and subsequent horizontal phase jumps in the picture. The rise time of the transients must be prolonged by GR smoothing networks so that they are slower than the response time of the phase control loop. Typical circuits which may cause load transients are:

1) e.h.t. circuits;
2) vertical deflection circuits;
3) sound circuits.

Fig.4 summarises the auxiliary supply and base drive considerations.

Under certain conditions (see Ref.1), it is possible for one extreme of the duty factor range required by the SMPS to extend beyond the allowed limit dictated by the drive requirements of the horizontal deflection transistor: the horizontal deflection transistor cannot then be driven by the SMPS unless the required duty factor range is shifted in the appropriate direction. Such a shift can be achieved by using a tapped choke as shown in Fig.5. In this circuit arrangement, the duty factor of the SMPS switching waveform is given by:

$$\delta = \frac{nV_o}{V_i - V_o(1-n)} \; . \qquad \ldots(11)$$

The required turns ratio for the two sections of the choke winding for any value of duty factor is given by:

$$n = \frac{\delta}{1-\delta}\left(\frac{V_i}{V_o} - 1\right) \; . \qquad \ldots(12)$$

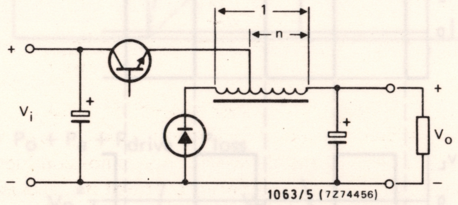


Fig.5 — Tapped choke to shift the required duty factor range of the SMPS

A DESIGN SPECIFICATION

The specification given below relates to an SMPS for a colour tv receiver using the 20AX deflection system. A block diagram of the power distribution to the various parts of the receiver is given in Fig.6.

The vertical deflection circuit, E-W correction stage, and the sound output stage (class-B with shunt stabiliser) are supplied by a rectified scan voltage derived from a secondary winding on the line output transformer. The shunt stabiliser in the sound output stage prevents audio modulation of the picture. Alternatively, a class-B audio stage could be supplied from an auxiliary winding on the SMPS choke. In this case care must be exercised to provide adequate filtering of rapid audio load variations. For ease of servicing, the small-signal stages are fed from an auxiliary winding on the SMPS output choke. The 225V supply for the RGB output stages is obtained by adding a rectified scan voltage of about 60V to the main SMPS output voltage.

Typical requirements for a 220V television power supply are:

mains voltage range (220V –15%, +20%)	187 to 265V a.c.
main output voltage (V_o)	165V d.c.
minimum instantaneous load on main output (no beam current) ($P_{o(min)}$)	70W
maximum instantaneous load on main output (white bar) ($P_{o(max)}$)	130W
losses in the SMPS components small-signal auxiliary load	10W
small-signal auxiliary load (P_a = 16V, 0.4A)	7W
base drive auxiliary load ($P_{drive} = 4V \times 1.4A \times (1-\delta)$)	4W
stabilisation of main output, better than	1%
ripple level 50Hz/100Hz hum, better than	0.2%
switching frequency (T = 64μs)	15 625Hz

Duty factor range

The power supply must operate from r.m.s. mains voltages of between 187V and 265V. With a ripple voltage of about 25V peak-to-peak, the instantaneous d.c. input voltage (V_i) range will be about 235V to 370V.

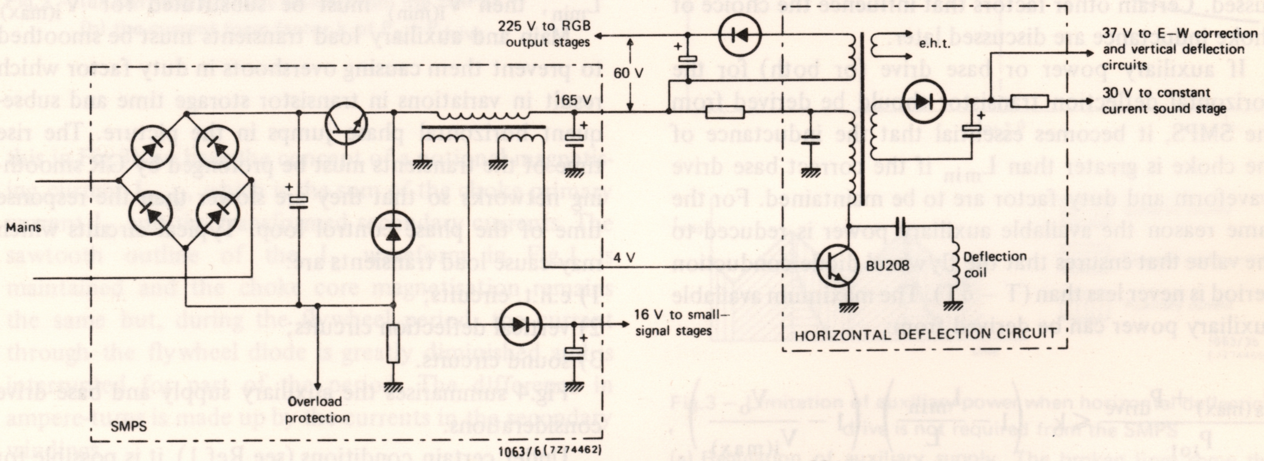

225 V to RGB output stages
60 V
165 V
Mains
4 V
16 V to small-signal stages
Overload protection
SMPS
e.h.t.
37 V to E–W correction and vertical deflection circuits
30 V to constant current sound stage
BU208
Deflection coil
HORIZONTAL DEFLECTION CIRCUIT
1063/6 (7Z74462)

Fig.6 — Power distribution in a television receiver using the 20AX deflection system. To minimise the power requirements, use can be made of very efficient circuits such as class-B video output and switched-mode vertical deflection output. If a class-B sound output stage is used, the required supply voltage may be derived from the SMPS

Since the main output voltage is 165V, the duty factor ($\delta = V_o/V_i$) must vary between 0.45 and 0.70 to compensate for input voltage variations. The requirements of the horizontal deflection output transistor, which is driven in the non-simultaneous mode, dictate a maximum drive duty factor range of 0.35 to 0.72 (Ref.1). The duty factor range to stabilise the SMPS output voltage against input voltage variations falls slightly outside the range dictated by the requirements of the horizontal deflection output transistor. It therefore appears to be necessary to shift the duty factor range by using a tapped choke. However, the increased storage time of the horizontal output transistor at minimum mains voltage, combined with the storage time of the horizontal efficiency diode, slightly increases the permitted duty factor range (Ref.1). It is thus not necessary to use a tapped choke in this instance.

Precautions must be taken to ensure that the horizontal deflection output transistor will not be forward-biased during the flyback period while a fault exists. To this end, a negative-going gating pulse must be applied to the base of either the SMPS drive transistor or the horizontal deflection transistor. The former method can only be used if the core of the choke remains unsaturated one flyback period after the initiation of the overload protection (see the description of pin 6 of the TDA2581 in the Appendix).

Output choke

The base of the horizontal deflection output transistor is driven by a current derived from a secondary winding on the SMPS output choke. To ensure that the drive current is always well defined, the inductance of the choke must be sufficient to ensure that the flywheel diode conduction period is not reduced to less than $T(1-\delta)$. By inserting $V_{i(max)}$ = 370V and k = 0.7 in Eq.10, it can be calculated that this condition will exist in the specified power supply if the inductance of the choke is not less than about $1.5L_{min}$.

From the equation for L_{min} given in Fig.2, a value of 5.3mH can be calculated for L_{min} in the specified power supply. The minimum inductance for the choke is therefore:

$$1.5 \times 5.3 \times 10^{-3} \simeq 8\text{mH}.$$

If the inductance of the choke is very much higher than this minimum value, considerable energy will be stored in its core when the SMPS output transistor is conducting. When the transistor is cut-off by either the remote control or the overload protection circuit, the horizontal deflection transistor will remain forward-biased until all the stored energy has been dissipated. This would result in a very high peak collector current in the horizontal deflection output transistor. (The actual current depends on such values as the capacitance of the S-correction capacitor, the saturation level of the line output transformer, and the resistance of the flashover protection resistor; see Ref.1.)

Overload protection voltage

Three methods of sensing an SMPS overload are shown in Fig.7. If the inductance of the choke is not much greater than L_{min}, the slope of the SMPS output transistor collector current will be greater than it would be with a high-inductance choke. Consequently, the collector current increase during the delay of the overload protection circuit is increased as shown in Fig.8. In such a case, the input voltage for the overload protection circuit cannot be developed across a resistor connected in series with the flywheel diode without risking excessive collector current in the SMPS output transistor or saturation of the core of the choke before the overload protection circuit comes into operation. The maximum momentary load on the SMPS is:

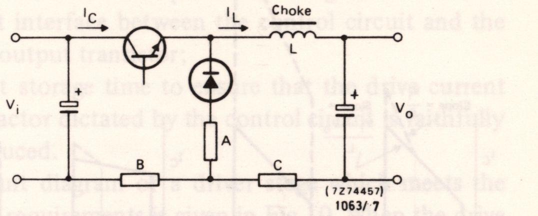


Fig.7 — Positioning of overload protection sensing resistor. A prevents forward-biasing of deflection transistor during the flyback period because the flywheel diode is not conducting; there is a danger of high peak I_C during overload if L is close to L_{min} or if core of L is saturated. B senses I_C, but the waveform across the sensing resistor may cause radiation problems. C senses I_L, and the smoother waveform across the resistor minimises radiation

$$P_{tot(max)} = P_{o(max)} + P_{loss} + P_a + P_{drive},$$

$$= 130 + 10 + 7 + 4 = 151\text{W}. \qquad \ldots(13)$$

With a choke inductance of 9mH and a minimum d.c. input voltage of 235V, the maximum peak collector current for the SMPS output transistor is:

$$I_{C(pk)} = \frac{V_oT}{2L}\left(1 - \frac{V_o}{V_{i(min)}}\right) + \frac{P_{tot(max)}}{V_o},$$

$$= \frac{165 \times 64 \times 10^{-6}}{18 \times 10^{-3}}\left(1 - \frac{165}{235}\right) + \frac{151}{165},$$

$$= 1.1\text{A}. \qquad \ldots(14)$$

In addition, during slow-start, small current overshoots

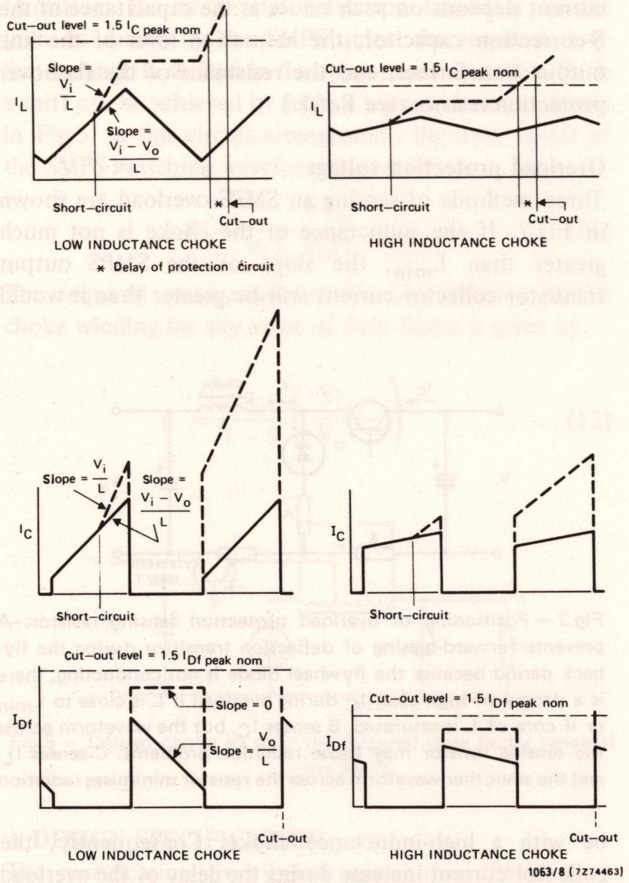


Fig.8 – Increase of collector current through the SMPS output transistor during an output short-circuit. The full line is the normal condition and the broken line is the overload condition
(a) Sensing choke current or collector current to detect overload
(b) Sensing flywheel diode current to detect overload

of about 200mA can occur, resulting in a total maximum peak collector current of 1.3A. The value of the overload sensing resistor must be such that the overload protection circuit is triggered at collector currents above this level (Ref.2). To allow for tolerances, the overload protection level chosen for the specified circuit is 1.6A.

Output stage

To ensure that the operating load line of the SMPS output transistor remains within the safe operating area (SOAR – see Refs.3 and 4) and to ensure correct base drive waveforms, it is necessary to incorporate passive components in the circuit. These components influence the behaviour of the circuit during the turn-off and turn-on periods of the SMPS output transistor.

When the SMPS output transistor is turned off, the inductive load causes the collector-emitter voltage to increase rapidly until it is clamped by the flywheel diode. The slope of this voltage is determined by the inductance of the choke and by the parasitic capacitance in the circuit. In practice, the maximum voltage is reached long before the collector current has fallen to zero. Without some form of protection, the turn-off losses would be considerable and there would be a high risk of thermal runaway. The slope of the increasing collector-emitter voltage must therefore be limited to about 1000V/μs by connecting a capacitor in parallel with the flywheel diode. If it is assumed that all the collector current is taken over by the damping capacitor during the turn-off period, the required capacitance is given by:

$$C_{min} = \frac{I_{CM}}{dV/dt}. \qquad \ldots(15)$$

For a maximum peak collector current of 1.6A, this gives a minimum damping capacitance of 1.6nF. The capacitor will, however, introduce losses during turn-on which are given by:

$$P_{loss} = \frac{CV_i^2}{2T}. \qquad \ldots(16)$$

For this reason, although the capacitor helps to reduce interference radiated to the aerial and h.f. stages, its value must not be too high. A good compromise is a value of 3.3nF.

From Fig.9, it can be seen that, when the transistor is turned on, the flywheel diode remains conducting until its reverse recovery charge has been removed via the transistor. During the turn-on period, the following currents flow:

1) the current to remove the reverse recovery charge from the flywheel diode;
2) the current to charge the damping capacitor connected in parallel with the flywheel diode;
3) the current flowing into the load via the choke;
4) the current flowing through the (parasitic) collector capacitances, such as choke interwinding capacitances.

Unless the rise time for the collector current is prolonged, the transistor will dissipate considerable energy during the turn-on interval before it bottoms. This rise time of the collector current can be prolonged by using a small choke to provide a current-limiting impedance in the collector circuit of the transistor. A series-connected diode and resistor must be connected in parallel with the small choke to absorb the stored energy and thereby limit the peak voltage across the transistor at the instant when it turns off again.

The value of the resistor must be such that, when the transistor switches on again, it absorbs all the energy in the choke. A rule of thumb for the resistor value is:

$$R = 10L/T. \qquad \ldots(17)$$

However, because the required values are influenced by parasitic capacitances in the choke and flywheel diode and also by the base current of the transistor, they must be determined experimentally. This is done by choosing values that reduce the peak collector current at switch-on to a level that ensures that the transistor remains within area III of the published SOAR. Since the losses introduced by the inductor during turn-off are:

$$P_{loss} = \frac{LI^2_{pk}}{2T}, \qquad \ldots(18)$$

the value of the inductance should be limited. In the specified power supply, a value of 200μH is used for the current-limiting choke, and a value of 39Ω is used for the resistor. These values limit the overshoot to 1.6A (the overload protection level) × 39Ω = 62V. The maximum value for $V_{CE(pk)}$ is therefore 370 +62 = 432V.

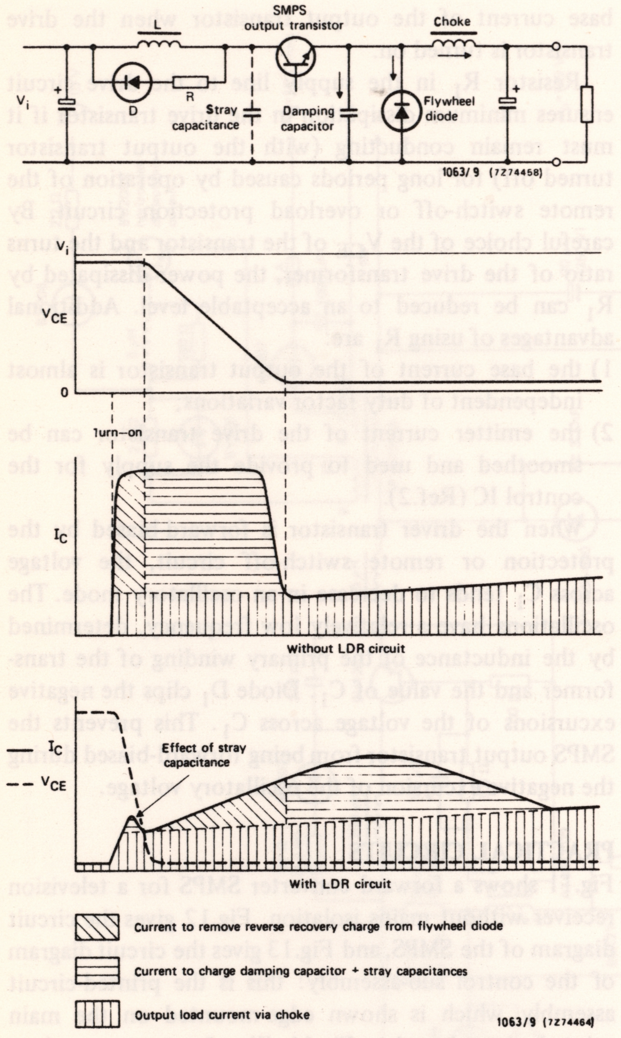


Fig.9 – Limiting the SMPS output transistor dissipation during turn-on

Driver stage

The SMPS output stage uses a high-voltage silicon npn transistor type BU126 which is specifically intended for use in television SMPS circuits. Turn-on losses must be minimised by ensuring that the drive circuit provides a fast-rising base current which maintains sufficient amplitude to ensure a low saturation voltage throughout the conduction period of this transistor. Turn-off losses must be minimised by ensuring that its reverse base current persists after its collector current starts to decrease. Other requirements for the driver stage are as follows:

1) the ability to operate satisfactorily within the range of specified mains voltages;
2) the ability to maintain the output transistor in the non-conducting state for long periods (operation of protection circuits or remote switch-off);
3) the provision of adequate current gain to ensure a correct interface between the control circuit and the SMPS output transistor;
4) a short storage time to ensure that the drive current duty factor dictated by the control circuit is faithfully reproduced.

A circuit diagram of a driver stage which meets the foregoing requirements is given in Fig.10. When the drive transistor ceases to conduct, forward base current is delivered to the output transistor by virtue of the energy stored in the core of the driver transformer. To ensure a short rise time for the base current, R_2 and C_2 in Fig.10 (which limit the ringing on the collector voltage waveform of the drive transistor) must underdamp the transformer.

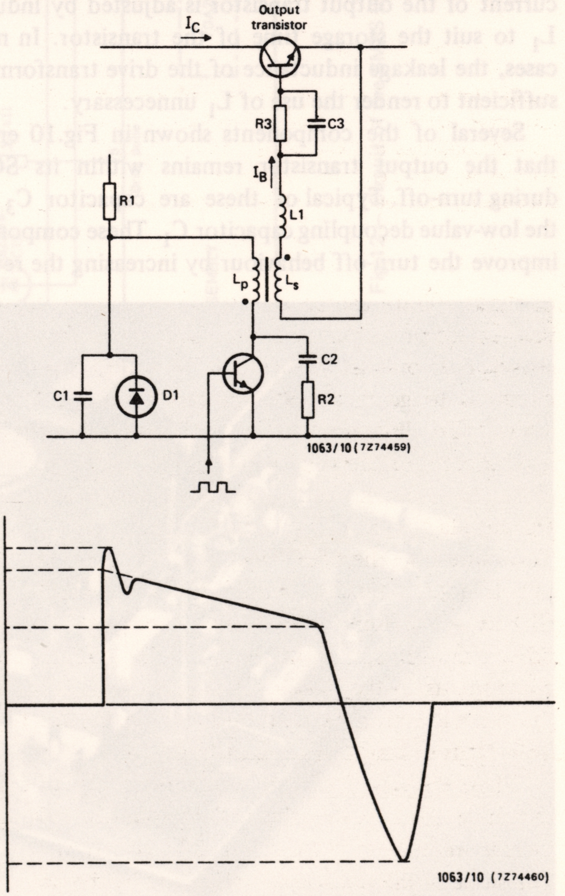


Fig.10 – Typical driver stage with base current waveform for the output transistor

This provides a degree of overshoot to compensate for the effect of the storage time adjustment inductor L_1. The rise time of the base current is further shortened by the effect of the speed-up network (R_3 and C_3) in the base circuit of the output transistor.

During the conduction period of the output transistor, its base current decreases to its final value ($I_{B(end)}$) at a rate dependent on the inductance of the secondary winding of the drive transformer (L_s). The base current reduction (ΔI_B) during the conduction period of the output transistor is given by:

$$\Delta I_B = I_{B(start)} - I_{B(end)}. \qquad \ldots (19)$$

The inductance of the secondary winding of the drive transformer must be high enough to prevent excessive base current reduction during the output transistor conduction period. The required inductance is:

$$L_s = \frac{(V_{BE} + I_B R_3)\delta T}{\Delta I_B}, \qquad \ldots (20)$$

where ΔI_B is the acceptable current reduction.

A typical value of inductance for the secondary winding of the drive transformer is 1mH.

During turn-off, the slope of the negative-going base current of the output transistor is adjusted by inductor L_1 to suit the storage time of the transistor. In many cases, the leakage inductance of the drive transformer is sufficient to render the use of L_1 unnecessary.

Several of the components shown in Fig.10 ensure that the output transistor remains within its SOAR during turn-off. Typical of these are capacitor C_3 and the low-value decoupling capacitor C_1. These components improve the turn-off behaviour by increasing the reverse base current of the output transistor when the drive transistor is turned on.

Resistor R_1 in the supply line to the drive circuit ensures minimum dissipation in the drive transistor if it must remain conducting (with the output transistor turned off) for long periods caused by operation of the remote switch-off or overload protection circuit. By careful choice of the V_{CE} of the transistor and the turns ratio of the drive transformer, the power dissipated by R_1 can be reduced to an acceptable level. Additional advantages of using R_1 are:

1) the base current of the output transistor is almost independent of duty factor variations;
2) the emitter current of the drive transistor can be smoothed and used to provide the supply for the control IC (Ref.2).

When the driver transistor is forward-biased by the protection or remote switch-off circuit, the voltage across C_1 tends to decrease in an oscillatory mode. The oscillations have a relatively low frequency, determined by the inductance of the primary winding of the transformer and the value of C_1. Diode D_1 clips the negative excursions of the voltage across C_1. This prevents the SMPS output transistor from being forward-biased during the negative excursion of the oscillatory voltage.

PRACTICAL CIRCUITS

Fig.11 shows a forward converter SMPS for a television receiver without mains isolation. Fig.12 gives the circuit diagram of the SMPS, and Fig.13 gives the circuit diagram of the control sub-assembly: this is the printed-circuit assembly which is shown edge-mounted on the main printed-wiring board in Fig.11. Waveforms measured on the SMPS are shown in Figs.14 to 16.

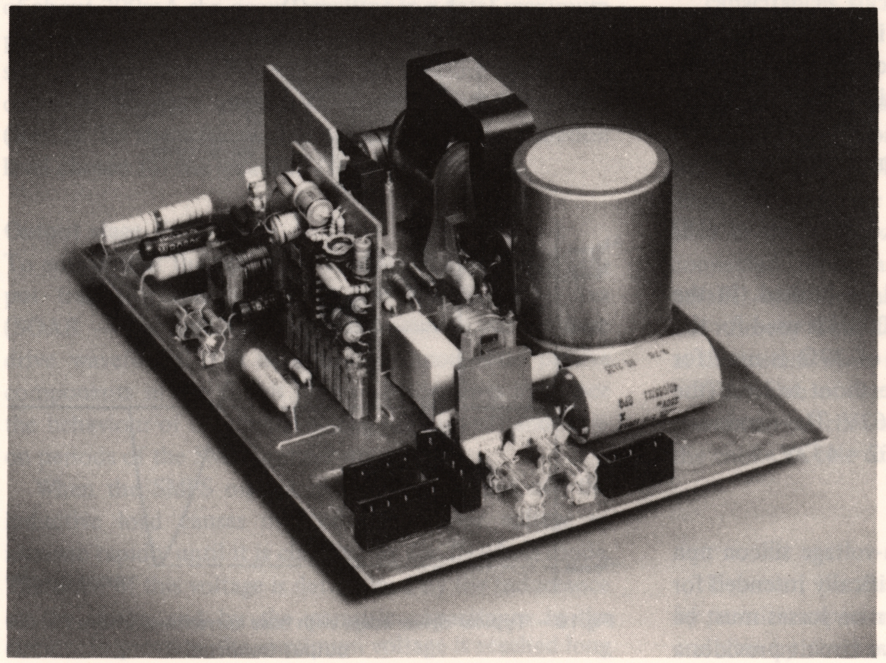


Fig.11 – A forward converter SMPS

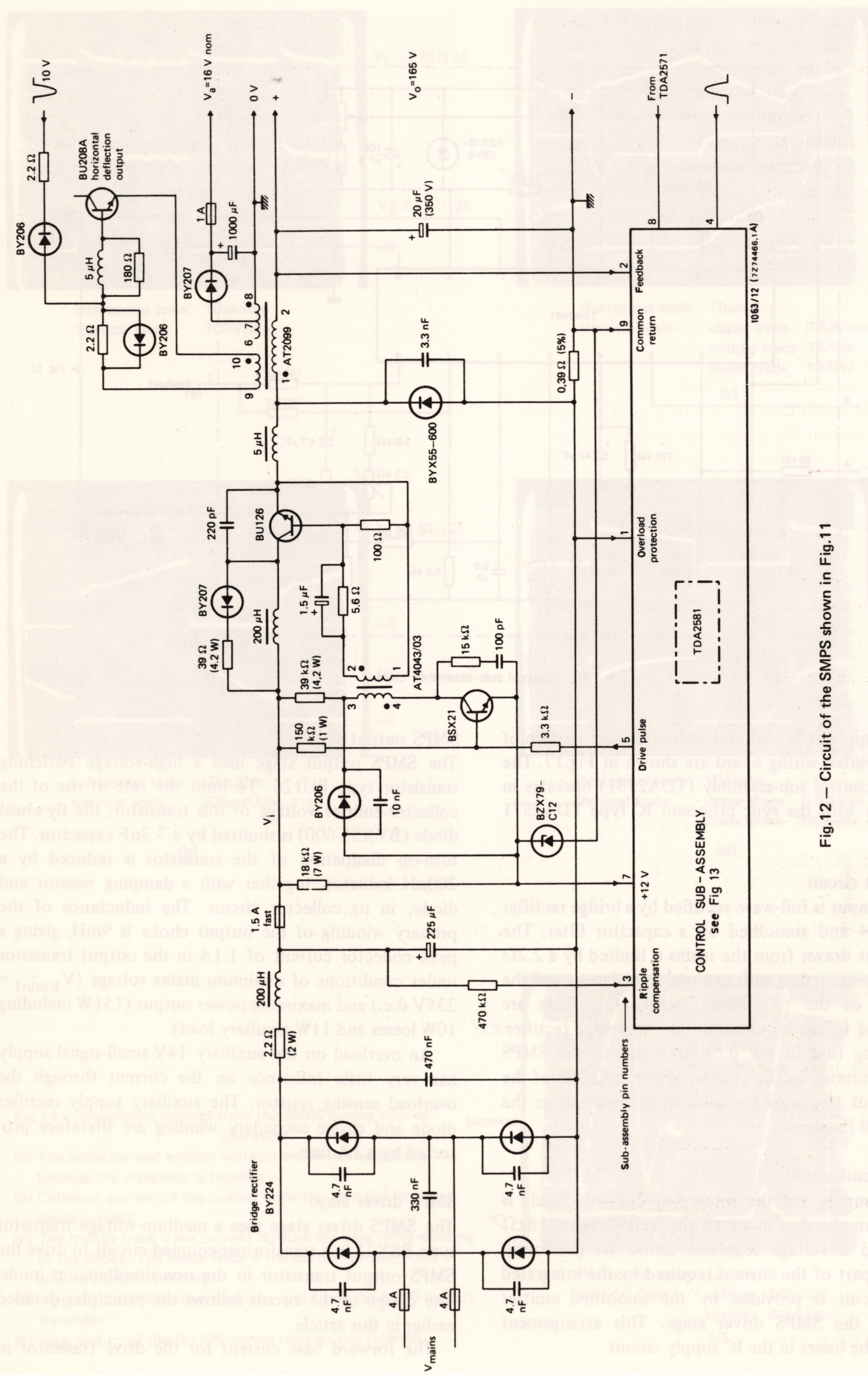

10 V
2.2 Ω
BY206
BU208A horizontal deflection output
5 μH
180 Ω
2.2 Ω
BY206
BY207
1 A
1000 μF
V_a=16 V nom
0 V
+ 1
20 μF (350 V)
V_o=165 V
AT2099
3.3 nF
BYX55-600
5 μH
220 pF
BU126
100 Ω
BY207
200 μH
1.5 μF
5.6 Ω
39 Ω (4.2 W)
39 kΩ (4.2 W)
AT4043/03
15 kΩ
100 pF
BSX21
3.3 kΩ
150 kΩ (1 W)
BY206
10 nF
V_1
18 kΩ (7 W)
BZX79-C12
1.5 A fast
225 μF
200 μH
470 kΩ
2.2 Ω (2 W)
470 nF
4.7 nF
4.7 nF
4.7 nF
4.7 nF
330 nF
4 A
4 A
V_{mains}
Bridge rectifier BY224
0.39 Ω (5%)
Common return
Feedback
From TDA2571
Overload protection
TDA2581
Drive pulse
+12 V
Ripple compensation
CONTROL SUB-ASSEMBLY see Fig 13
Sub-assembly pin numbers
1063/12 (7Z74466.1A)

Fig.12 – Circuit of the SMPS shown in Fig.11

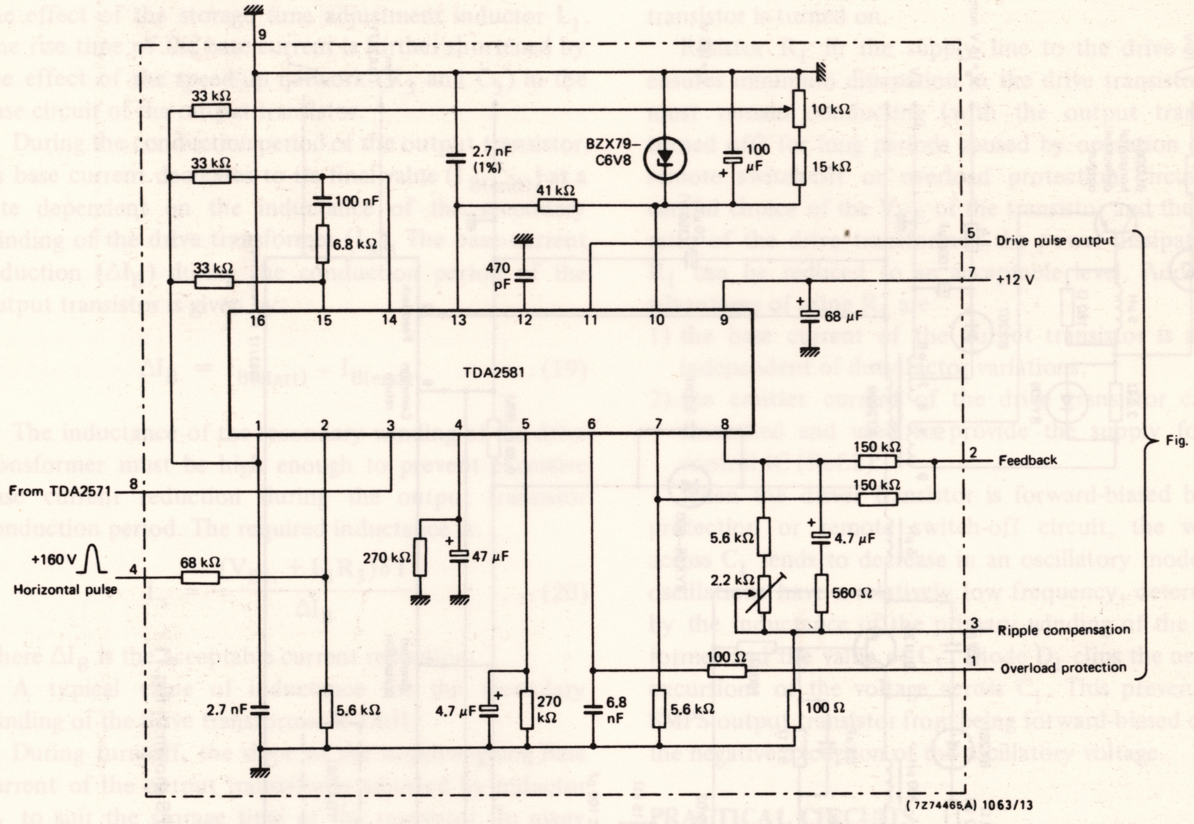


Fig.13 – Control sub-assembly circuit

The component layout and etched copper pattern of the main printed-wiring board are shown in Fig.17. The IC on the control sub-assembly (TDA2581) operates in conjunction with the sync processor IC type TDA2571 (see Ref.2).

Mains input circuit

The mains input is full-wave rectified by a bridge rectifier type BY224 and smoothed by a capacitor filter. The peak current drawn from the mains is limited by a 2.2Ω resistor in conjunction with external impedances and the impedance of the r.f.i. filter. Slow-acting fuses are incorporated in the input circuit to the bridge rectifier. A fast-acting fuse in the d.c. input line to the SMPS limits the currents in the receiver if the collector of the SMPS output transistor becomes short-circuited to the common rail (heatsink).

Control circuit supply

The 12V supply for the integrated control circuit is derived from the d.c. input to the SMPS via an 18kΩ resistor and a voltage regulator diode. As previously explained, part of the current required by the integrated control circuit is provided by the smoothed emitter current of the SMPS driver stage. This arrangement minimises the losses in the IC supply circuit.

SMPS output stage

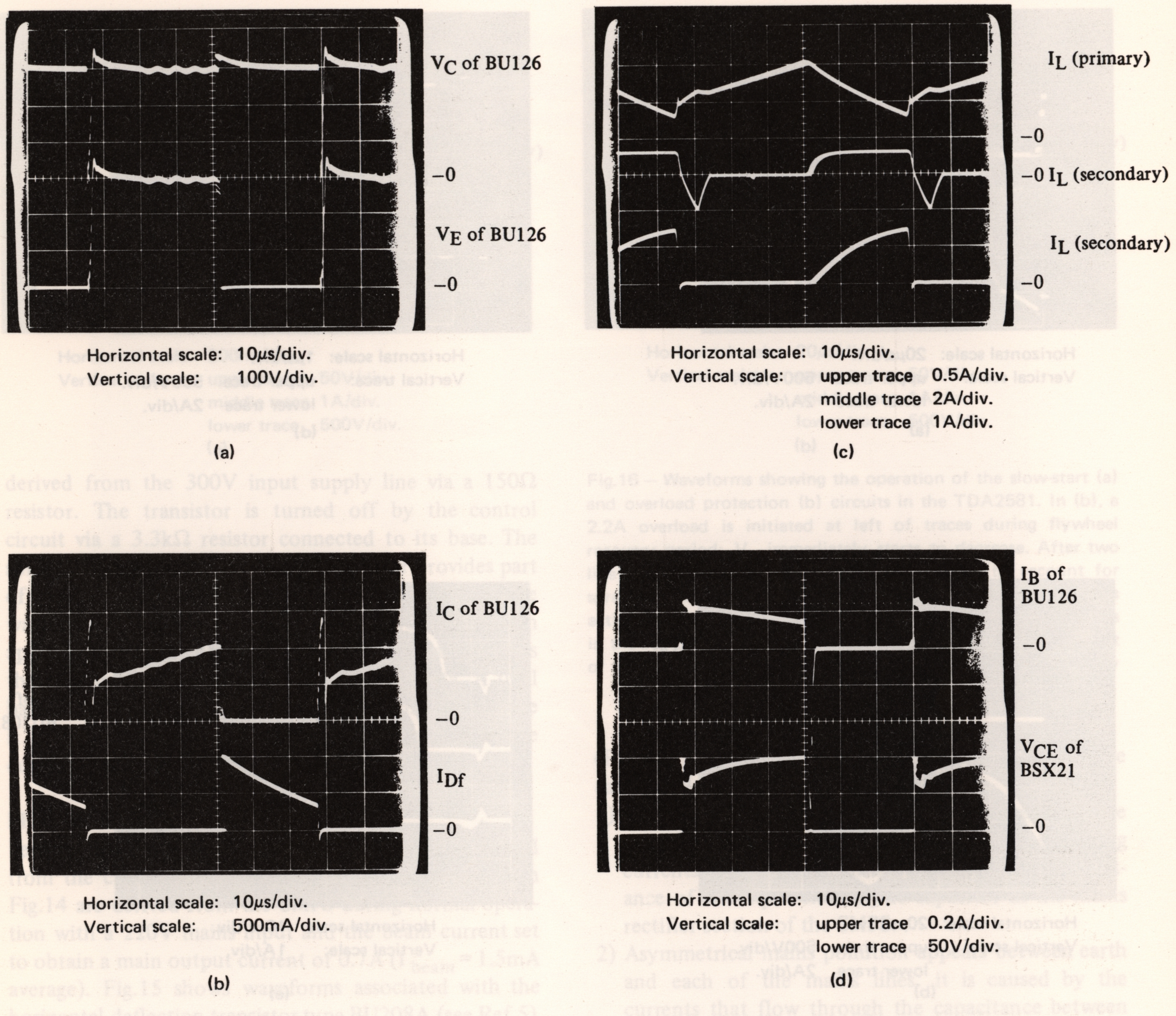
The SMPS output stage uses a high-voltage switching transistor type BU126. To limit the rate of rise of the collector-emitter voltage of this transistor, the flywheel diode (BYX55-600) is shunted by a 3.3nF capacitor. The turn-on dissipation of the transistor is reduced by a 200µH inductor, together with a damping resistor and diode, in its collector circuit. The inductance of the primary winding of the output choke is 9mH, giving a peak collector current of 1.1A in the output transistor under conditions of minimum mains voltage ($V_{i(min)}$ = 235V d.c.) and maximum power output (151W including 10W losses and 11W auxiliary load).

An overload on the auxiliary 14V small-signal supply has very little influence on the current through the overload sensing resistor. The auxiliary supply rectifier diode and choke secondary winding are therefore protected by a 1A fuse.

SMPS driver stage

The SMPS driver stage uses a medium-voltage transistor type BSX21 in a transformer-coupled circuit to drive the SMPS output transistor in the non-simultaneous mode. The design of the circuit follows the principles detailed earlier in this article.

The forward base current for the drive transistor is



Horizontal scale: 10µs/div.
Vertical scale: 100V/div.

(a)

Horizontal scale: 10µs/div.
Vertical scale: upper trace 0.5A/div.
middle trace 2A/div.
lower trace 1A/div.

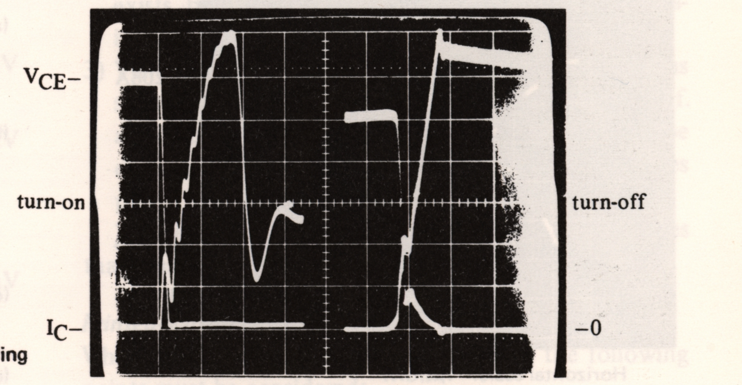
(c)

Horizontal scale: 10µs/div.
Vertical scale: 500mA/div.

(b)

Horizontal scale: 10µs/div.
Vertical scale: upper trace 0.2A/div.
lower trace 50V/div.

(d)



Horizontal scale: 1µs/div.
Vertical scale: voltage 50V/div.
current 0.2A/div.

(e)

Fig.14 – Waveforms derived from the SMPS during normal operation

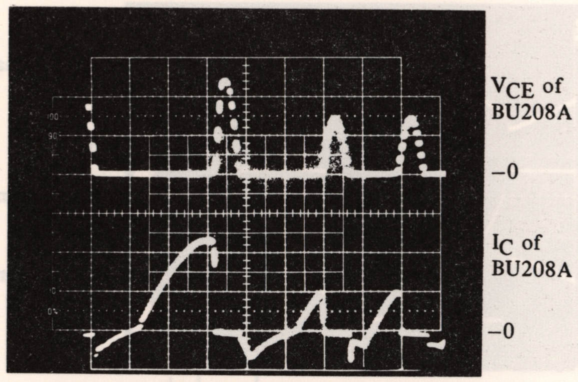
(a) The collector and emitter voltages are shown separately because the transistor is floating

(b) Collector current of the output transistor and the flywheel diode current

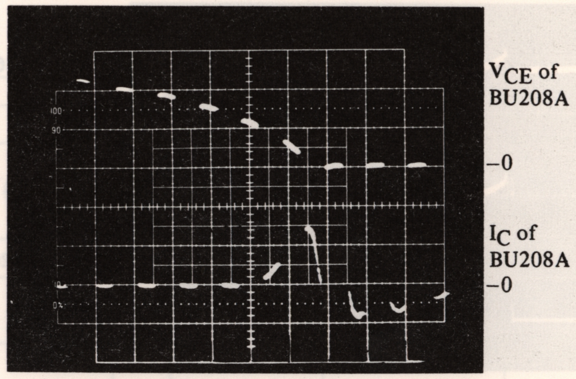
(c) The middle trace is the current through the base drive winding of the choke. The lower trace is the current through the auxiliary power winding.

(d) V_{CE} of the SMPS drive transistor and I_B of the SMPS output transistor

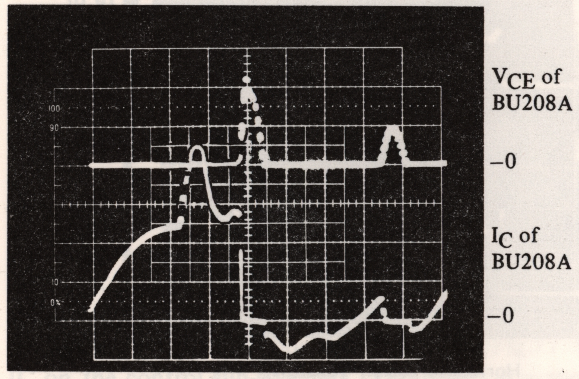
(e) V_{CE} and I_C of the BU126 during turn-on and turn-off



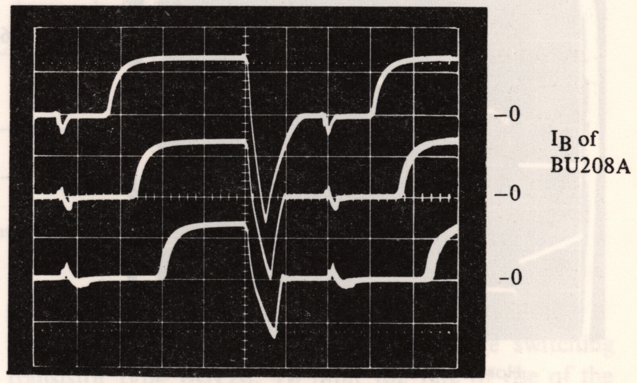
Horizontal scale: 20μs/div.
Vertical scale: upper trace 500V/div.
lower trace 2A/div.
(a)



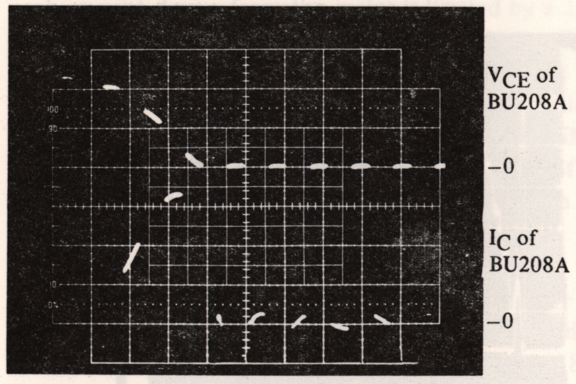
Horizontal scale: 1μs/div.
Vertical trace: upper trace 500V/div.
lower trace 2A/div.
(d)



Horizontal scale: 20μs/div.
Vertical scale: upper trace 500V/div.
lower trace 2A/div.
(b)



Horizontal scale: 10μs/div.
Vertical scale: 1A/div.
(e)



Horizontal scale: 1μs/div.
Vertical scale: upper trace 500V/div.
lower trace 2A/div.
(c)

Fig.15 – Waveforms associated with the horizontal deflection transistor

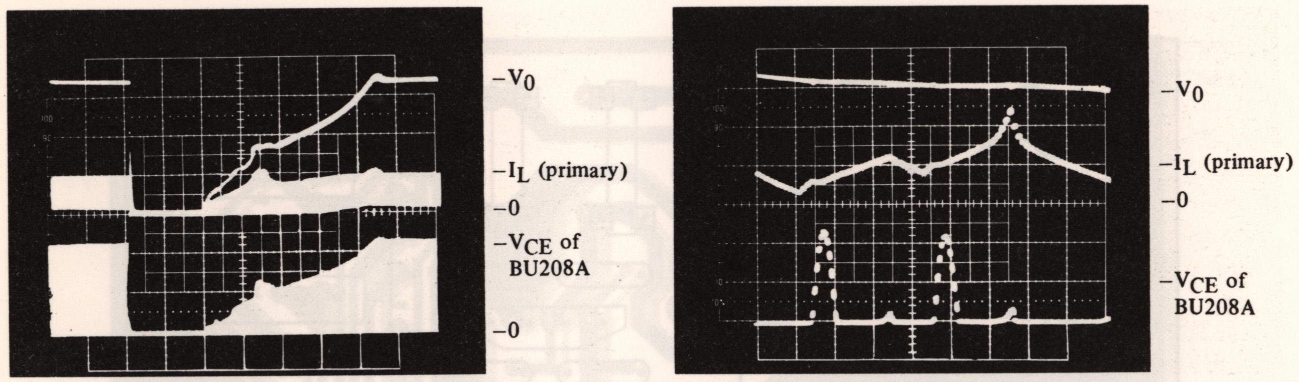
(a) Effect of false triggering of overload protection during the flyback pulses. The collector current reaches 4.6A. Spurious uncontrolled switching of the deflection transistor continues for a few cycles after the base drive has ceased

(b) As (a) but overload initiated at the most critical time (when the energy stored in the choke is maximum). The forward drive lasts longer than in (a) and the collector current reaches a peak of 9A because of the behaviour of the E-W correction circuit. A non-repetitive peak current of 10A is allowed (Ref.3)

(c) Initiation of overload at middle of flyback pulse without gating the output transistor base. The combination of I_C and V_{CE} falls outside the SOAR

(d) As (c) but with gating of the output transistor base. The combination of I_C and V_{CE} falls within the SOAR.

(e) Base drive current for BU208A for V_{mains} = 220V + 10% (upper trace), 220V – 15% (lower trace), and 220V (middle trace)



Horizontal scale: 200ms/div.
Vertical scale: upper trace 50V/div.
middle trace 1A/div.
lower trace 500V/div.
(a)

Horizontal scale: 20μs/div.
Vertical scale: upper trace 50V/div.
middle trace 1A/div.
lower trace 500V/div.
(b)

Fig.16 – Waveforms showing the operation of the slow-start (a) and overload protection (b) circuits in the TDA2581. In (b), a 2.2A overload is initiated at left of traces during flywheel recovery period: V_O immediately starts to decrease. After two line periods, the choke current reaches 2A (to account for spreads; nominal level is 1.6A) and the protection circuit is activated. The choke current increases to 2.3A because of delays in the IC, drive transistor and output transistor. Note the onset of saturation of the choke core at about 1.5A choke primary current

derived from the 300V input supply line via a 150Ω resistor. The transistor is turned off by the control circuit via a 3.3kΩ resistor connected to its base. The smoothed emitter current of the transistor provides part of the 12V supply for the control circuit (Ref.2). The waveforms in Fig.14 show that the current waveform applied to the base of the SMPS output transistor meets the requirements published in the BU126 data. A final base current $I_{B(end)}$ = 140mA has been chosen because it corresponds with a collector current equal to the cut-out level of the protection circuit, that is 1.6A.

PERFORMANCE

Performance figures and waveforms have been derived from the circuit shown in Fig.12. Waveforms shown in Fig.14 are derived from the SMPS during normal operation with a 220V mains input and the beam current set to obtain a main output current of 0.7A (I_{beam} = 1.5mA average). Fig.15 shows waveforms associated with the horizontal deflection transistor type BU208A (see Ref.5). Fig.16 shows waveforms of the operation of the slow-start and overload protection circuits in the TDA2581. Regulation and ripple performance are indicated below.

Main output (V_o = 165V nominal):	
ΔV_o for V_{mains} = 187V to 265V	100mV
ΔV_o for d.c. input (V_i) ripple of 20V peak-to-peak at 100Hz	120mV
output impedance at I_o = 0.7A	0.4Ω
Auxiliary output (V_a = 16V nominal):	
ΔV_a for V_{mains} = 187V to 265V	800mV
output impedance at I_a = 0.45A	2Ω

Interference

The high-frequency switching of an SMPS, and the presence of high-level alternating voltages and currents, cause a certain amount of interference to be generated (Ref.1). The interference can be divided into three categories.

1) Symmetrical mains pollution appears between the mains input lines and is generated by the switching currents flowing through the equivalent series resistance of the input electrolytic capacitor in the mains rectifier section of the SMPS.
2) Asymmetrical mains pollution appears between earth and each of the mains lines: it is caused by the currents that flow through the capacitance between earth and components carrying high a.c. voltages. This type of interference is most pronounced in mains-isolated supplies because of the high impedance that exists between the primary winding and the mains-isolating secondary winding of the output choke.
3) Visible interference is caused by radiated spurious signals being injected into either the tuner or the i.f. amplifier circuits or both. The main cause of this type of interference is the high dI/dt of the current pulses passes by the switching diodes and transistors.

The following points give a brief guide to the measures that must be taken to reduce SMPS interference.

Printed-wiring board layout

When designing the printed-wiring board, the following points must be considered:

1) minimisation of the length of the circuit loop comprising the input electrolytic capacitor, the SMPS output transistor, and the flywheel diode;

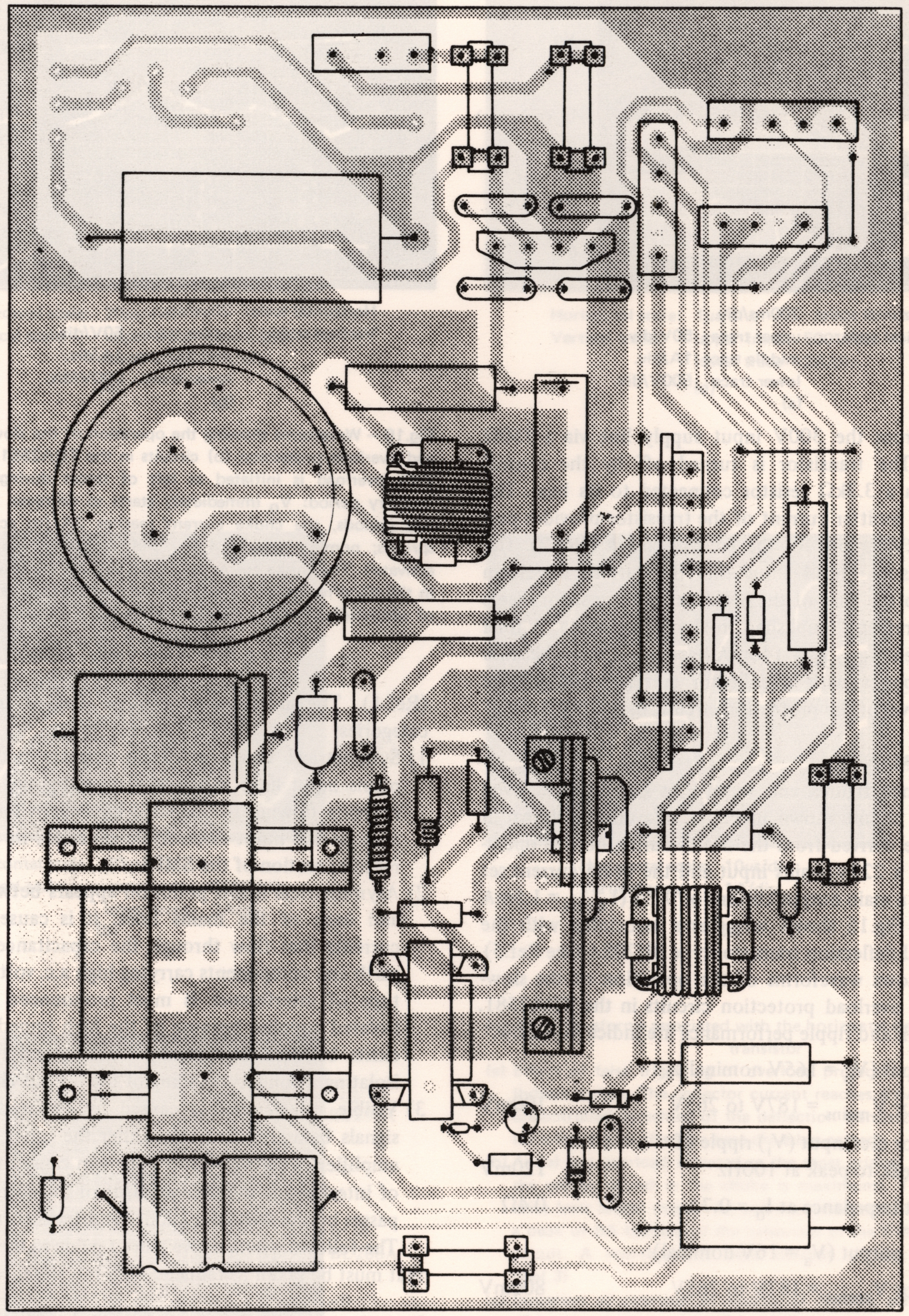


Fig.17a — Component side of the printed-wiring board for the circuit of Fig.12 (actual size)

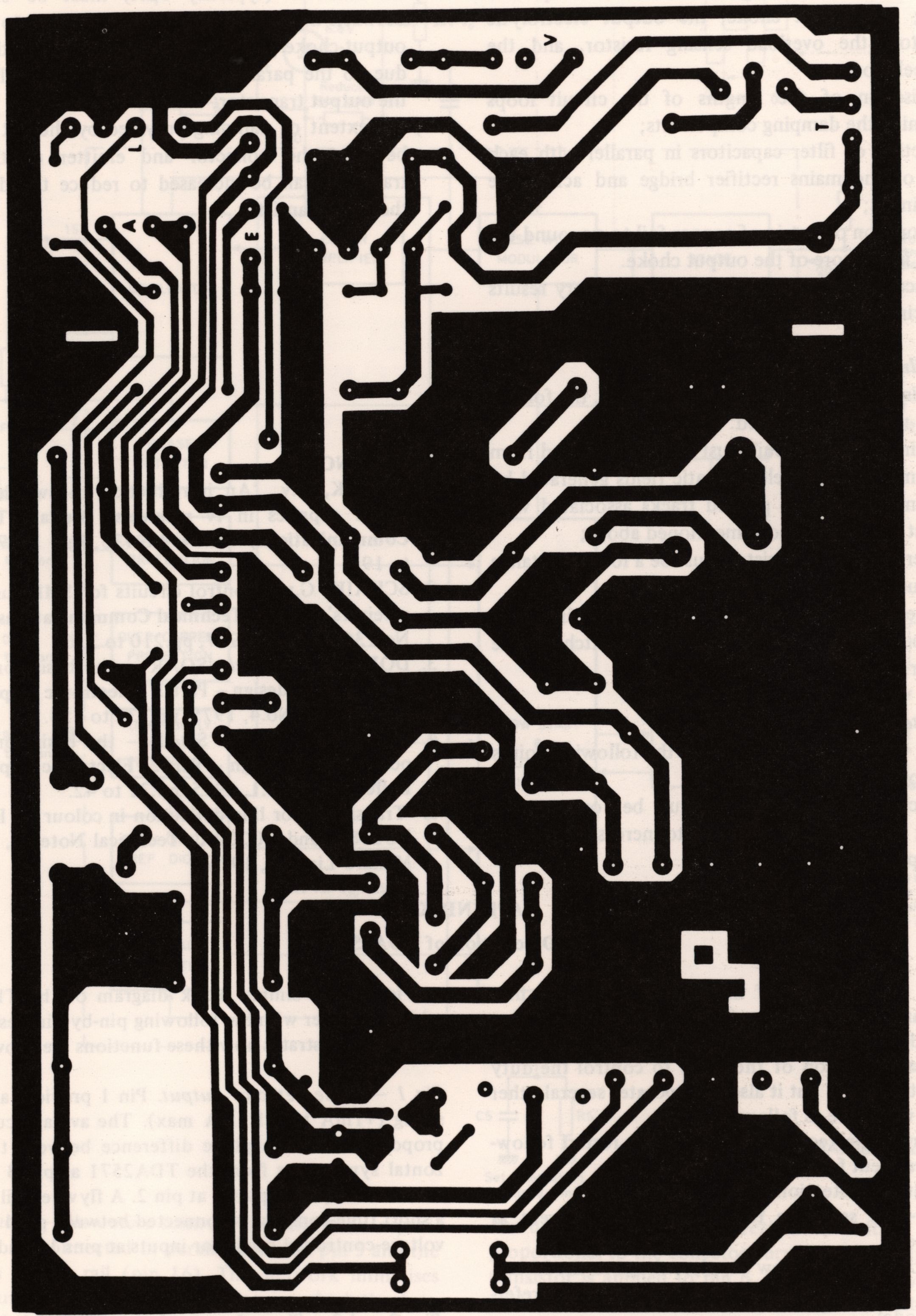


Fig.17b — Copper side of the printed-wiring board for the circuit of Fig.12 (actual size)

2) minimisation of the length of the circuit loop comprising the output choke, the output electrolytic capacitor, the overload sensing resistor, and the flywheel diode;
3) minimisation of the lengths of the circuit loops containing the damping components;
4) connection of filter capacitors in parallel with each diode of the mains rectifier bridge and across the mains input;
5) incorporation of a strip of copper foil to surround the air gap in the core of the output choke.

A typical layout which has given satisfactory results with the circuit of Fig.12 is shown in Fig.17.

Mains pollution

To assist in the reduction of mains pollution, the following points must be considered:
1) the mains rectifier circuit must be well separated from electromagnetic and electrostatic fields generated by the components and printed tracks associated with the first two circuit loops mentioned above;
2) the overload sensing resistor must be a low-inductance type, such as carbon or glass-sealed wire;
3) the filter capacitor connected across the mains input must be located close to the mains switch of the receiver.

Visible interference

In dealing with visible interference, the following points must be considered:
1) a capacitor (typically 3.3nF) must be connected in parallel with the flywheel diode to increase the dV/dt at this point;
2) an inductor (typically $5\mu H$) must be connected between the emitter of the output transistor and the output-choke primary winding to decrease the dI_c/dt due to the parasitic capacitance of the collector of the output transistor;
3) the extent of damping provided by the CR network between the collector and emitter of the drive transistor can be increased to reduce the dV_c/dt of the drive transistor.

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3. DORN, W.M., *et al*, 'SOAR – the basis for reliable power circuit design – Part 1', **Electronic Applications Bulletin**, 32, No.4, 1975, pp.137 to 153.
4. DORN, W.M., *et al*, 'SOAR – the basis for reliable power circuit design – Part 2', **Electronic Applications Bulletin**, 33, No.1, 1975, pp.31 to 42.
5. 'Transistors for line deflection in colour tv: BU207A, BU208A, and BU209A', Technical Note 38, TP1546, Mullard Limited, 1976.

APPENDIX

Brief Description of TDA2581

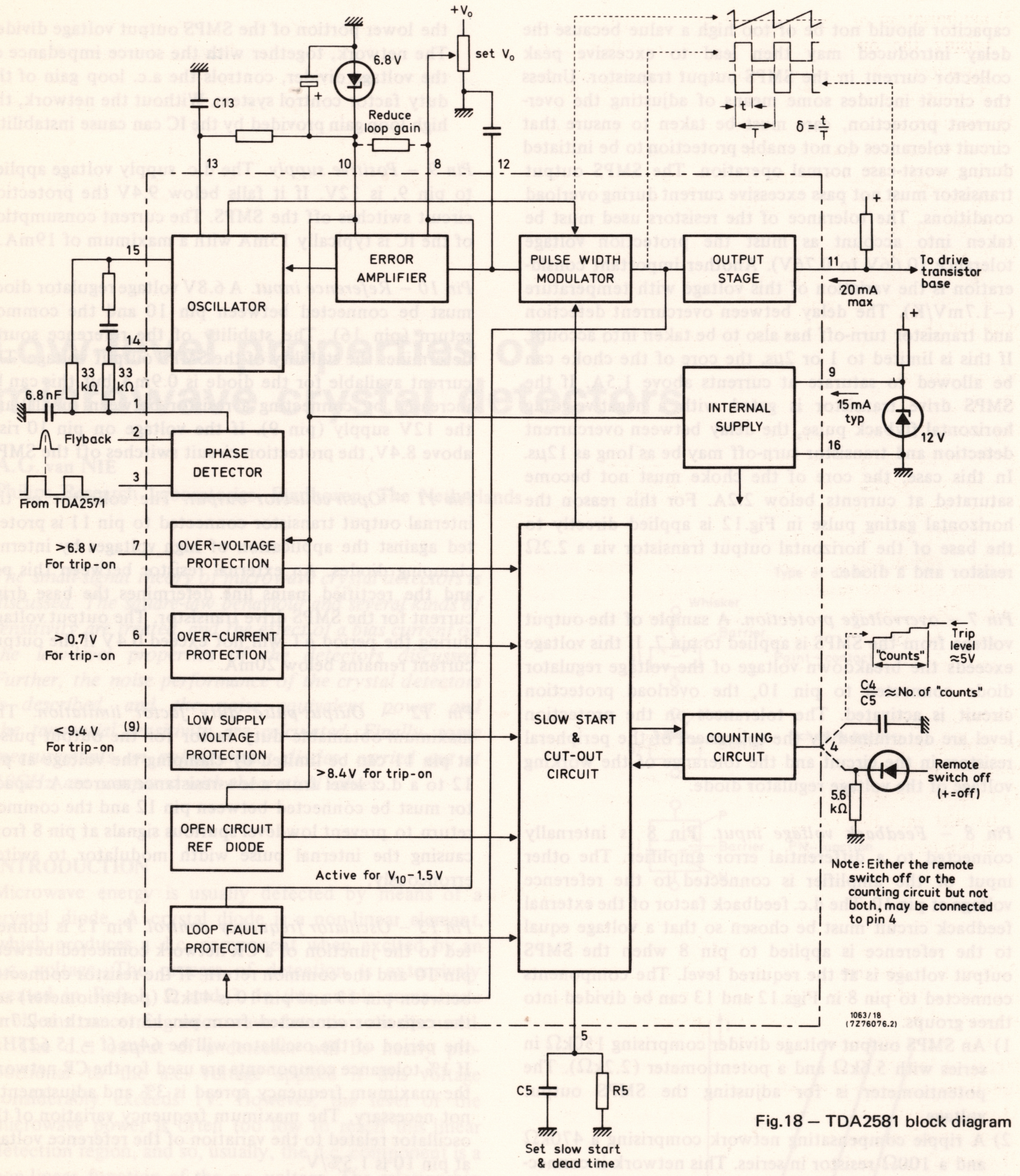
Although a description of the TDA2581 is given in a previous article in this series (Ref.2), a brief description is included here for the sake of completeness.

The main function of the IC is to control the duty factor of the SMPS but it also incorporates several other functions which are as follows:
1) overcurrent protection with automatic restart following a transient fault;
2) overvoltage protection;
3) a slow-start sequence to prevent inrush current at switch-on;
4) protection against a low supply voltage to the IC and against an open-circuit or disconnected voltage reference diode;
5) protection in the event of a fault in the feedback loop during slow-start;
6) a rapid-response phase control loop that compensates the SMPS drive pulses for delays in the horizontal deflection circuit, thereby permitting horizontal deflection drive to be derived from the SMPS.

Fig.18 is a simple block diagram of the TDA2581 which, together with the following pin-by-pin description of the IC, illustrates how these functions are provided.

Pin 1 – Phase detector output. Pin 1 provides a current swing (+1mA to −1.5mA max). The average current is proportional to the phase difference between the horizontal sync pulses from the TDA2571 at pin 3 and the horizontal flyback pulses at pin 2. A flywheel filter with a short time-constant is connected between pin 1 and the voltage-controlled oscillator inputs at pins 14 and 15.

Pins 2 and 3 – Phase detector inputs. Noise-free reconstituted horizontal sync pulses from the TDA2571 are connected to the phase detector input at pin 3. Picture phase information for the phase detector is connected to pin 2; the input to pin 2 can either be a flyback pulse, or a spike obtained from a small toroid the core of which is saturated by the horizontal deflection current.



+V₀
set V₀
6.8V
C13
Reduce loop gain
13
10
8
12
15
14
1
2
3
7
6
(9)
11
9
16
4
5
ERROR AMPLIFIER
OSCILLATOR
33 kΩ
33 kΩ
6.8nF
Flyback
PHASE DETECTOR
From TDA2571
>6.8V For trip-on
OVER-VOLTAGE PROTECTION
>0.7V For trip-on
OVER-CURRENT PROTECTION
<9.4V For trip-on
LOW SUPPLY VOLTAGE PROTECTION
>8.4V for trip-on
OPEN CIRCUIT REF DIODE
Active for V₁₀−1.5V
LOOP FAULT PROTECTION
PULSE WIDTH MODULATOR
OUTPUT STAGE
t
T
δ = t/T
To drive transistor base
20mA max
INTERNAL SUPPLY
15mA typ
12V
SLOW START & CUT-OUT CIRCUIT
COUNTING CIRCUIT
"Counts"
Trip level ≈5V
C4/C5 ≈ No. of "counts"
Remote switch off (+=off)
5.6 kΩ
Note: Either the remote switch off or the counting circuit but not both, may be connected to pin 4
1063/18 (7Z76076.2)
C5
R5
Set slow start & dead time

Fig.18 – TDA2581 block diagram

Pins 4 and 5 – Slow-start control. A resistor and capacitor must be connected in parallel between pin 5 and the common return rail (pin 16). This network minimises inrush current by controlling the rate at which the duty factor of the SMPS drive pulses increases from a small value to its operating value after switch-on. The value of the capacitor connected to pin 4 determines the number of slow-start repetitions that can occur before the SMPS output is permanently switched off in the event of a persistent fault. Pin 4 can also be used for remote switch-off.

Pin 6 – Overcurrent protection. A voltage which is proportional to the collector current of the SMPS output transistor is applied to pin 6. The voltage may be either positive or negative, and the operating level is about 0.7V. For current operation, the operating levels are $+2\mu A$ and $-100\mu A \pm 30\%$. In the circuit shown in Figs.12 and 13, the SMPS output current flows through a 0.39Ω resistor in the supply return line. The voltage across this resistor is fed back to pin 6 via a CR filter with a time-constant of $1\mu s$. The CR filter prevents premature operation of the protection circuit by interference spikes. The filter capacitor should not be of too high a value because the delay introduced may then lead to excessive peak collector current in the SMPS output transistor. Unless the circuit includes some means of adjusting the over-current protection, care must be taken to ensure that circuit tolerances do not enable protection to be initiated during worst-case normal operation. The SMPS output transistor must not pass excessive current during overload conditions. The tolerance of the resistors used must be taken into account as must the protection voltage tolerance (0.66V to 0.76V). Another important consideration is the variation of this voltage with temperature (−1.7mV/K). The delay between overcurrent detection and transistor turn-off has also to be taken into account. If this is limited to 1 or 2µs, the core of the choke can be allowed to saturate at currents above 1.5A. If the SMPS drive transistor is gated with a negative-going horizontal flyback pulse, the delay between overcurrent detection and transistor turn-off may be as long as 12µs. In this case, the core of the choke must not become saturated at currents below 2.2A. For this reason the horizontal gating pulse in Fig.12 is applied directly to the base of the horizontal output transistor via a 2.2Ω resistor and a diode.

Pin 7 – overvoltage protection. A sample of the output voltage from the SMPS is applied to pin 7. If this voltage exceeds the breakdown voltage of the voltage regulator diode connected to pin 10, the overload protection circuit is activated. The tolerances on the protection level are determined by the tolerances of the peripheral resistors in the circuit and the tolerance of the working voltage of the voltage regulator diode.

Pin 8 – Feedback voltage input. Pin 8 is internally connected to a differential error amplifier. The other input of the amplifier is connected to the reference voltage at pin 10. The d.c. feedback factor of the external feedback circuit must be chosen so that a voltage equal to the reference is applied to pin 8 when the SMPS output voltage is at the required level. The components connected to pin 8 in Figs.12 and 13 can be divided into three groups.

1) An SMPS output voltage divider comprising 150kΩ in series with 5.6kΩ and a potentiometer (2.2kΩ). The potentiometer is for adjusting the SMPS output voltage.
2) A ripple compensating network comprising a 470kΩ and a 100Ω resistor in series. This network is connected across the rectified mains to provide feedforward which is used in the IC to counteract ripple in the SMPS output.
3) A CR network comprising a 4.7µF capacitor in series with a 560Ω resistor, and connected in parallel with the lower portion of the SMPS output voltage divider. The network, together with the source impedance of the voltage divider, controls the a.c. loop gain of the duty factor control system. Without the network, the high loop gain provided by the IC can cause instability.

Pin 9 – Positive supply. The d.c. supply voltage applied to pin 9, is 12V. If it falls below 9.4V the protection circuit switches off the SMPS. The current consumption of the IC is typically 15mA with a maximum of 19mA.

Pin 10 – Reference input. A 6.8V voltage regulator diode must be connected between pin 10 and the common return (pin 16). The stability of the reference source determines the stability of the SMPS output voltage. The current available for the diode is 0.9mA but this can be increased by connecting a resistor between pin 10 and the 12V supply (pin 9). If the voltage on pin 10 rises above 8.4V, the protection circuit switches off the SMPS.

Pin 11 – Open-collector output. The collector of the internal output transistor connected to pin 11 is protected against the application of high voltages by internal clamping diodes. An external resistor between this pin and the rectified mains line determines the base drive current for the SMPS drive transistor. The output voltage during the period δT will not exceed 0.4V if the output current remains below 20mA.

Pin 12 – Output-pulse duty factor limitation. The maximum-obtainable duty factor for the output pulses at pin 11 can be limited by clamping the voltage at pin 12 to a d.c. level from a low-resistance source. A capacitor must be connected between pin 12 and the common return to prevent low-level spurious signals at pin 8 from causing the internal pulse width modulator to switch erroneously.

Pin 13 – Oscillator frequency control. Pin 13 is connected to the junction of a CR network connected between pin 10 and the common return. If the resistor connected between pin 13 and pin 10 is 41kΩ (potentiometer) and the capacitor connected from pin 13 to earth is 2.7nF, the period of the oscillator will be 64µs (f = 15 625Hz). If 1% tolerance components are used for the CR network, the maximum frequency spread is 3% and adjustment is not necessary. The maximum frequency variation of the oscillator related to the variation of the reference voltage at pin 10 is 1.5%/V.

Pins 14 and 15 – Flywheel filter. See pin 1.

Pin 16 – Common return. The negative side of the 12V supply connected to pin 9 must be connected to pin 16.

Low-level properties of microwave crystal detectors

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The small-signal theory of microwave crystal detectors is discussed. The square-law behaviour and several kinds of sensitivity are treated, and the effect of a bias current on the low-level properties of the detectors discussed. Further, the noise performance of the crystal detectors is described, and the noise equivalent power and the tangential sensitivity are calculated. Finally, some measurements on point-contact diodes, carried out at 10GHz, are compared with theoretical values.

INTRODUCTION

Microwave energy is usually detected by means of a crystal diode. A crystal diode is a non-linear element, which produces a d.c. component when excited by an a.c. voltage. The process of detection is extensively treated in Refs.1, 2, and 3. In this article some basic problems concerning microwave detection are discussed.

The d.c. output of a detector will be nearly proportional to the a.c. voltage applied if this voltage considerably exceeds 1V. However, the level of the microwave power is often too low to reach this linear detection region, and so, usually, the d.c. component is a non-linear function of the a.c. voltage. The relationship between the d.c. component and the a.c. voltage is governed by the 'I V' characteristic of the diode. Fig.1 shows this characteristic schematically for some of the most important types of diode, a short description of each being given in the following.

The point-contact diode consists of a metal whisker

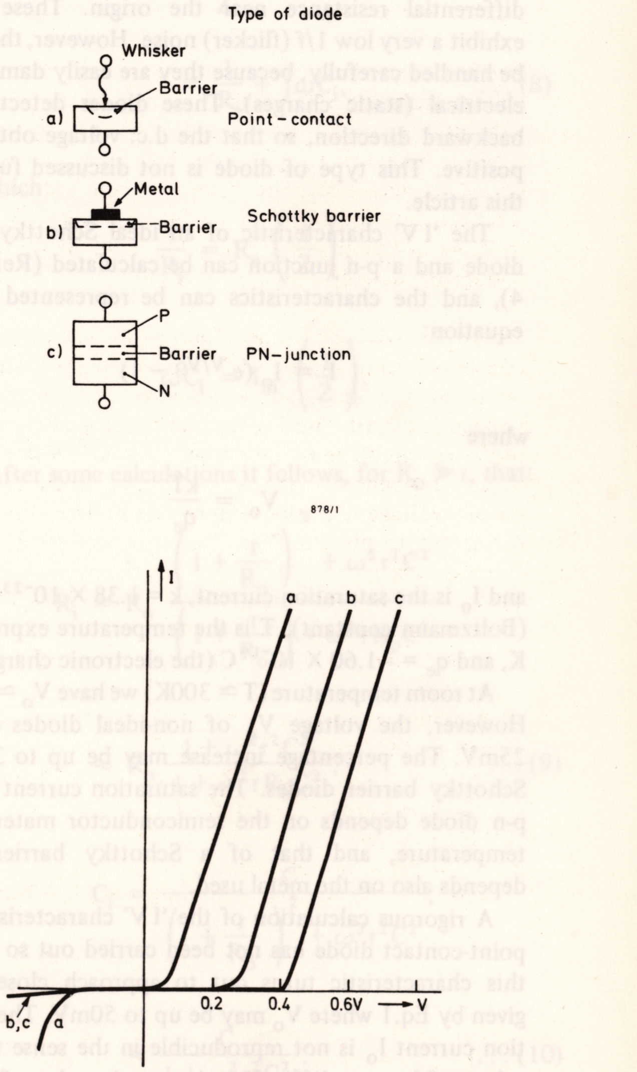

Fig. 1 — 'IV' characteristics of several silicon diodes

This article is a revised and updated version of that first published in 'Electronic Measuring and Microwave Notes', 1970/1, N.V. Philips, Eindhoven, The Netherlands.

in contact with a piece of semiconductor material such as germanium or silicon. The barrier, being the active area between the metal and the semiconductor material, acts as a diode. This type of detector can be used for detecting microwaves with frequencies up to 300GHz.

The metal semiconductor diode (Schottky barrier diode) is also employed for detection of microwaves. In these detectors a metal spot on top of the crystal is used instead of a whisker. This diode is more reliable than a point-contact diode, but its high differential resistance dV/dI near the origin is a disadvantage which is discussed later.

A semiconductor crystal made of n-type and p-type material can also, in principle, be used for detecting microwaves: the junction between the n-type and p-type material is the active area. This type of diode is not very suitable for detecting microwaves, and is more suited for use as a variable capacitor (varactor) or as a tunnel diode at these frequencies.

Also, we should mention the backward diodes, in which specially doped material is applied to lower the differential resistance near the origin. These diodes exhibit a very low 1/f (flicker) noise. However, they must be handled carefully, because they are easily damaged by electrical (static charges). These diodes detect in the backward direction, so that the d.c. voltage obtained is positive. This type of diode is not discussed further in this article.

The 'I V' characteristic of an ideal Schottky barrier diode and a p-n junction can be calculated (Refs.1 and 4), and the characteristics can be represented by the equation:

$$I = I_o\left(e^{V/V_o} - 1\right) \qquad \ldots(1)$$

where

$$V_o = \frac{kT}{q_e}$$

and I_o is the saturation current, $k = 1.38 \times 10^{-23}$ J/degC (Boltzmann constant), T is the temperature expressed in K, and $q_e = -1.60 \times 10^{-19}$C (the electronic charge).

At room temperature ($T \simeq 300$K) we have $V_o \simeq 25$mV. However, the voltage V_o of non-ideal diodes exceeds 25mV. The percentage increase may be up to 30% for Schottky barrier diodes. The saturation current I_o of a p-n diode depends on the semiconductor material and temperature, and that of a Schottky barrier diode depends also on the metal used.

A rigorous calculation of the 'I V' characteristic of a point-contact diode has not been carried out so far, but this characteristic turns out to approach closely that given by Eq.1 where V_o may be up to 50mV. The saturation current I_o is not reproducible in the sense that the values of I_o may differ from item to item by a factor of 10. After detection, the barrier voltage V consists of the a.c. voltage V_{ac} to be detected and the d.c. voltage V_{dc} obtained, that is:

$$V = V_{ac} + V_{dc}.$$

The corresponding diode currents, satisfying the equation:

$$I = I_{ac} + I_{dc},$$

can be derived from the 'IV' characteristic of the diode. The a.c. voltage V_{ac} can be compared with V_o, and we can then use the term 'low level' to mean the voltage range

$$|V_{ac}| \ll V_o.$$

For low levels the current I is mainly determined by the first terms of the series expansion of exp (V/V_o), and we obtain as an approximation:

$$I_{ac} + I_{dc} \approx I_o\left\{\frac{V_{ac} + V_{dc}}{V_o} + \frac{1}{2}\left(\frac{V_{ac} + V_{dc}}{V_o}\right)^2\right\} \qquad \ldots(2)$$

The relation between the d.c. components is then:

$$I_{dc} \approx I_o\left\{\frac{V_{dc}}{V_o} + \frac{\overline{V_{ac}^{\,2}}}{2V_o^{\,2}} + \frac{V_{dc}^{\,2}}{2V_o^{\,2}}\right\}. \qquad \ldots(3)$$

For $V_{dc} = 0$ we have the d.c. short-circuit current:

$$(I_{dc})_{V_{dc}=0} = \frac{1}{2} I_o \frac{\overline{V_{ac}^{\,2}}}{V_o^{\,2}}, \qquad \ldots(4)$$

and for $I_{dc} = 0$ we get, by neglecting higher order terms, the d.c. open-circuit voltage:

$$(V_{dc})_{I_{dc}=0} = -\frac{1}{2}\frac{\overline{V_{ac}^{\,2}}}{V_o}. \qquad \ldots(5)$$

Obviously, the d.c. current is proportional to the a.c. power at low levels of detection. This performance is known as the square-law behaviour of the diode. As the upper limit for this behaviour we may take the a.c. voltage at which $V_{ac} = V_o$.

The equivalent circuit of the crystal diode is shown in Fig.2. The a.c. barrier voltage V_{ac} is in general smaller than the a.c. voltage applied to the diode because of the barrier capacitance C and the spreading resistance r in the semiconductor material. The differential or barrier resistance R_o at the origin is given by.

$$R_o = \left[\left(\frac{dI}{dV}\right)_{V=0}\right]^{-1} = \frac{V_o}{I_o}. \qquad \ldots(6)$$

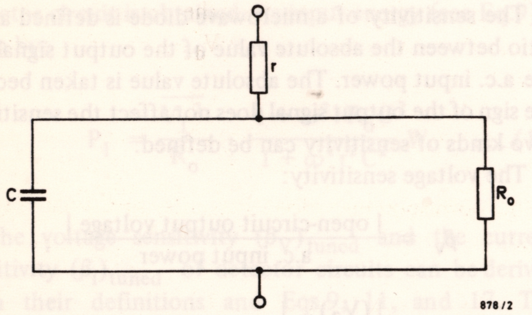

Fig.2 – Equivalent circuit of a crystal diode. R_o is the differential resistance, C the barrier capacitance, and r the spreading resistance in the semiconductor material

In general, the barrier resistance R_o is high compared with the series resistance. The crystal is mounted in a cartridge which introduces a parasitic inductance in series with, and a capacitance in parallel with, the crystal. To simplify the calculations these parasitic impedances are ignored.

SIMPLIFIED EQUIVALENT CIRCUIT OF THE DETECTOR

An a.c. detector can be composed of a diode, a highpass filter, and a lowpass filter, as shown schematically in Fig.3. The two filters separate the a.c. energy at the input from the d.c. energy at the output of the detector. With microwaves, a simple capacitor and a coil (or microwave choke) can be used for the highpass and lowpass filter respectively. In most cases, the effect of the capacitance on the a.c. signal and the resistance of the coil on the d.c. signal can be neglected, and at low signal level the a.c. impedance of the detector circuit is hardly dependent on the d.c. impedance connected to its output, so the detector circuit may be simplified to a 2-port with an a.c. input circuit separated from a d.c. output circuit, as in Fig.4. Under these conditions the input impedance is determined by the crystal impedance:

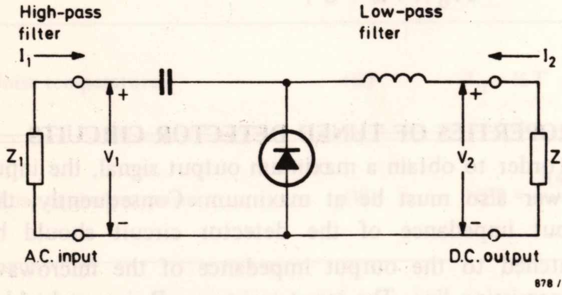

Fig.3 – Simplified detector circuit. Z_1 is the characteristic impedance of the transmission line and Z_2 the impedance of the d.c. measuring instrument

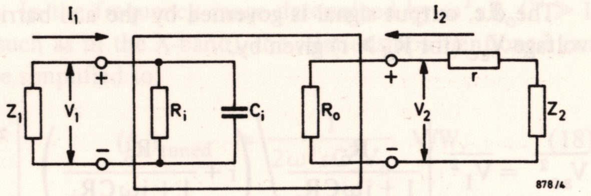

Fig.4 – Detector circuit represented by a 2-port

$$Z = r + \frac{R_o}{1 + j\omega C R_o}. \qquad \ldots(7)$$

For power calculations it is convenient to regard Z as a parallel circuit with resistance R_i and capacitance C_i. We thus have:

$$Y = \frac{1}{Z},$$

$$= \frac{1}{R_i} + j\omega C_i, \qquad \ldots(8)$$

in which:

$$\frac{1}{R_i} = R_e\left(\frac{1}{Z}\right),$$

and,

$$\omega C_i = I_m\left(\frac{1}{Z}\right).$$

After some calculations it follows, for $R_o \gg r$, that:

$$R_i = R_o \frac{\left(1 + \frac{r}{R_o}\right)^2 + \omega^2 r^2 C^2}{\left(1 + \frac{r}{R_o}\right) + \omega^2 r R_o C^2},$$

$$\approx R_o \frac{1 + \omega^2 r^2 C^2}{1 + \omega^2 r R_o C^2}; \qquad \ldots(9)$$

and:

$$C_i = \frac{C}{\left(1 + \frac{r}{R_o}\right)^2 + \omega^2 r^2 C^2},$$

$$\approx \frac{C}{1 + \omega^2 r^2 C^2}. \qquad \ldots(10)$$

The d.c. output signal is governed by the a.c. barrier voltage V_{ac} (for $R_o \gg r$) given by:

$$\overline{V_{ac}^{\ 2}} = \overline{V_1^{\ 2}} \left| \frac{R_o}{1 + j\omega CR_o} \bigg/ \left(r + \frac{R_o}{1 + j\omega CR_o} \right) \right|^2$$

$$\approx \frac{\overline{V_1^{\ 2}}}{1 + \omega^2 r^2 C^2}, \qquad \ldots (11)$$

where V_1 is the input voltage. From this equation it follows that the barrier voltage V_{ac} decreases with increasing frequency, as already stated in the introduction. The cut-off frequency f_c is given by the relationship:

$$\omega_c rC = 2\pi f_c rC = 1. \qquad \ldots (12)$$

However, f_c will be often lowered by the parasitic impedances due to the cartridge. Nevertheless, the actual cut-off frequency of a normal microwave diode far exceeds 10GHz, and so, up to that frequency, we have $\omega rC \ll 1$.

At low levels, the d.c. output circuit of the detector can be represented by a virtual d.c. current source with internal resistance R_o (see Fig.5). The series resistance r is assumed to be a (small) part of the d.c. load, and so the barrier resistance R_o can be taken as the d.c. output impedance. The source current I_{dc} can be obtained from the short-circuit current given by Eq.4. From Eq.11 we get:

$$I_{dc} = I_o \frac{\overline{V_{ac}^{\ 2}}}{2V_o^{\ 2}},$$

$$= I_o \frac{\overline{V_1^{\ 2}}}{2(1 + \omega^2 r^2 C^2) V_o^{\ 2}}. \qquad \ldots (13)$$

With the assumed positive direction of current, the open-circuit voltage, given by:

$$(V_2)_{dc} = -I_2 R_o = -\frac{1}{2} I_o \frac{\overline{V_{ac}^{\ 2}}}{V_o^{\ 2}} R_o,$$

$$= -\frac{1}{2} \frac{\overline{V_{ac}^{\ 2}}}{V_o},$$

is thus in conformity with Eq.5.

SENSITIVITY OF MICROWAVE DIODES

The performance of microwave detectors is mainly determined by the diode characteristics V_o, I_o, r, and C. In addition to this data, the sensitivity of a detection circuit is often used as an indication of its quality.

The sensitivity of a microwave diode is defined as the ratio between the absolute value of the output signal and the a.c. input power. The absolute value is taken because the sign of the output signal does not affect the sensitivity. Two kinds of sensitivity can be defined.

1) The voltage sensitivity:

$$\beta_v = \frac{|\text{ open-circuit output voltage }|}{\text{a.c. input power}},$$

$$= \frac{|(V_2)_{oc}|}{P_1} \text{ V/W}. \qquad \ldots (14)$$

2) The current sensitivity:

$$\beta_i = \frac{|\text{ short-circuit output current }|}{\text{a.c. input power}}$$

$$= \frac{|(I_2)_{sc}|}{P_1} \text{ V/W}. \qquad \ldots (15)$$

The conversion loss of the detector is defined by:

$$L = 10 \log \left(\frac{\text{a.c. input power}}{\text{available d.c. output power}} \right),$$

$$= 10 \log \left(\frac{4P_1}{|(V_2)_{oc}(I_2)_{sc}|} \right) \text{dB}. \qquad \ldots (16)$$

The sensitivities and the conversion losses of tuned and broadband detector circuits are calculated below with the aid of the simplified detector circuit shown in Fig.5.

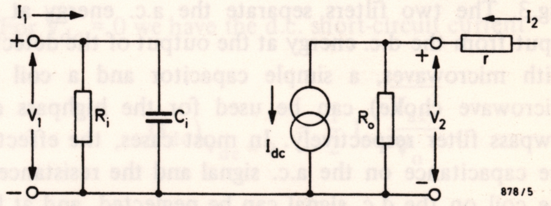

Fig.5 – Detector circuit where input and output circuits are separated. The current source

$$I_{dc} = \frac{I_o}{2V_o(1 + \omega^2 r^2 C^2)} \overline{V_1^{\ 2}}, \quad \text{provided that } r \ll R_o$$

PROPERTIES OF TUNED DETECTOR CIRCUITS

In order to obtain a maximum output signal, the input power also must be at maximum. Consequently, the input impedance of the detector circuit should be matched to the output impedance of the microwave transmission line. The input resistance R_i is matched by means of a transformer, and an inductive element compensates the input capacity C_i; in this way a tuned detector circuit is obtained. Its input energy (see Eq.9) is given by:

$$P_1 = \frac{\overline{V_1^{\ 2}}}{R_o} \cdot \frac{1 + \omega^2 rR_oC^2}{1 + \omega^2 r^2 C^2} \text{ W}. \qquad \ldots (17)$$

The voltage sensitivity $(\beta_V)_{tuned}$ and the current sensitivity $(\beta_i)_{tuned}$ of detector circuits can be derived from their definitions and Eqs.9, 11, and 17. The sensitivities are listed in Table 1.

In the frequency range determined by $\omega^2 rR_oC^2 \gg 1$ (such as in the X-band), the relationships mentioned can be simplified to:

$$(\beta_v)_{tuned} \approx \frac{1}{2\omega^2 rC^2 V_o} \text{ V/W}, \qquad \ldots (18)$$

$$(\beta_i)_{tuned} \approx \frac{1}{2\omega^2 rR_oC^2 V_o} \text{ A/W}. \qquad \ldots (19)$$

The sensitivity increases with decreasing spreading

TABLE 1 Definitions of Terms

		Tuned detector circuit $f \ll f_c$	Broadband detector circuit $Z_o \ll R_i$, $f \ll f_c$
Voltage sensitivity	(V/W)	$(\beta_v)_{tuned} = \frac{1}{2I_o(1 + \omega^2 rR_oC^2)}$	$(\beta_v)_{bb} = \frac{Z_o}{2V_o}$
Current sensitivity	(A/W)	$(\beta_i)_{tuned} = \frac{1}{2V_o(1 + \omega^2 rR_oC^2)}$	$(\beta_i)_{bb} = \frac{Z_o}{2R_oV_o}$
Conversion loss	(dB)	$(L)_{tuned} = 10 \log_e \left\{ 16 \frac{V_o^{\ 2}}{V_1^{\ 2}} (1 + \omega^2 rR_oC^2) \right\}$	$(L)_{bb} = 10 \log_e \left\{ 16 \frac{V_o^{\ 2}}{V_1^{\ 2}} \cdot \frac{R_o}{Z_o} \right\}$
Figure of Merit	$[W]^{-1/2}$	$(M)_{tuned} = \frac{1}{2(1 + \omega^2 rR_oC^2)\sqrt{(I_oV_o)}}$	$(M)_{bb} = \frac{Z_o}{2V_o\sqrt{R_o}}$
Voltage V_o	(V)	$V_o \geqslant \frac{kT}{q_e}$; $V_o \geqslant 25\text{mV}$ at $T = 300\text{K}$	
Bias current at working point V_d	(A)	$I_d = I_o \exp(V_d/V_o) = I_o + I_b$; I_b bias current	
Differential resistance	(Ω)	$R = \frac{V_o}{I_d} = \frac{V_o}{I_o + I_b} = \frac{R_o}{1 + I_b/I_o}$	
Cut-off frequency	(Hz)	$f_c = \frac{1}{2\pi rC}$	
Noise temperature	(K)	$T_d = \frac{1}{2}T \left(1 + \frac{I_o}{I_d} + \frac{2\alpha I_b}{f} \right)$	
Noise equivalent power	(W)	$\text{NEP} = \frac{\sqrt{(4kT_dFR\Delta f)}}{\beta_v} = \frac{\sqrt{(4kT_dFG\Delta f)}}{\beta_i} = \frac{\sqrt{(4kT_dF\Delta f)}}{\sqrt{(\beta_v\beta_i)}} = \frac{\sqrt{(4kT_dF\Delta f)}}{M}$	
Tangential sensitivity	(W)	TSS ≈ 5 × NEP (Gaussian distribution)	

resistance r, barrier capacitance C, and the voltage V_o. As stated, the minimum value of the voltage is about 25mV at 300K. Further, the sensitivity decreases by 6dB per octave in this frequency range. The voltage sensitivity $(\beta_V)_{tuned}$ is nearly independent of the saturation current I_o, whereas $(\beta_i)_{tuned}$ is proportional to I_o.

The conversion loss $(L)_{tuned}$ can be derived from the definition and Eqs.9 and 17. The conversion loss, given in Table 1 for frequencies $f \ll f_c$, increases with increasing frequency. Further, the level of the output power is significantly lower than that of the input power because $V_o \gg |V_1|$, and so the signal-to-noise ratio of the detector circuit is mainly determined by the output circuit.

PROPERTIES OF BROADBAND DETECTORS

In a tuned detector circuit, a transformer is applied for matching purposes. However, a transformer is frequency-dependent, and so not suitable for broadband detectors. Provided $R_i \gg Z_o$, the input resistance R_i of the detector circuit can be matched over a broadband to the characteristic impedance Z_o of the transmission line by connecting a resistance R_p in parallel with the input circuit.

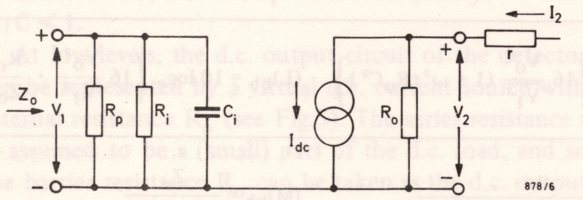

Fig.6 – Broadband microwave detector circuit. The resistor R_p equalises the input of the detector to the characteristic impedance Z_o. It is assumed that $R_i \gg Z_o$ (ωC_i)

The input resistance in Fig.6 must be equal to Z_o, and so R_p can be found from the equation:

$$Z_o = \frac{R_p R_i}{R_p + R_i}, \qquad \ldots(20a)$$

or:

$$R_p = \frac{Z_o R_i}{R_i - Z_o}. \qquad \ldots(20b)$$

Broadband detectors are usually employed in coaxial systems, with $Z_o = 50\Omega$, and so the input impedance R_i is much greater than Z_o up to 10GHz: consequently we may take $R_p = Z_o$. Likewise $[\omega C_i]^{-1}$ generally exceeds Z_o up to 10GHz, and so C_i should be compensated only in the high-frequency region.

The a.c. power P_c flowing through the coaxial cable, and the power P_l available for detection, are given by:

$$P_c = \frac{\overline{V_1{}^2}}{Z_o}, \qquad \ldots(21a)$$

and:

$$P_l = \frac{\overline{V_1{}^2}}{R_i}, \qquad \ldots(21b)$$

respectively. Consequently, the input power of the detector circuit is:

$$P_l = \frac{Z_o}{R_i} P_c. \qquad \ldots(22)$$

In tuned detector circuits, the total power P_c is available for detection, whereas in broadband detectors only the fraction (Z_o/R_i) of the total power is detected. Therefore, the sensitivity of a broadband detector in coaxial systems is reduced by that factor. The voltage sensitivity $(\beta_V)_{bb}$ and the current sensitivity $(\beta_i)_{bb}$ for the frequency range $0 \ll \omega^2 r^2 C^2 \ll 1$ are given in Table 1. The sensitivity of a broadband detector turns out to be nearly constant in the frequency range mentioned. Further, $(\beta_V)_{bb}$ is independent of the current I_o, whereas $(\beta_i)_{bb}$ is proportional to I_o.

EFFECT OF BIAS ON LOW-LEVEL DETECTION

The current sensitivity and the power loss of a microwave detector circuit are highly dependent on the differential resistance R_o and it can be shown that a low value of R_o implies a high performance. The differential resistance can be lowered by applying an external d.c. bias current I_b. The voltage V_d at the operating point can be obtained from the 'I V' characteristic.

$$I_b = I_o (e^{V_d/V_o} - 1), \qquad \ldots(23)$$

and so the differential resistance R is given by:

$$R = \left[\frac{dI_b}{dV_d}\right]^{-1} = \frac{V_o}{I_o} e^{-V_d/V_o} \qquad \ldots.(24)$$

The total current flowing through the diode is given by:

$$I_{ac} + I_{dc} + I_b = I_o \left[\exp\left\{(V_{ac} + V_{dc})/V_o\right\} \times \times \exp\left\{V_d/V_o\right\} - 1\right]. \qquad \ldots(25)$$

Eliminating the current I_b, Eq.25 becomes:

$$I_{ac} + I_{dc} = I_d \left[\exp\left\{(V_{ac} + V_{dc})/V_o\right\} - 1\right], \qquad \ldots(26)$$

with:

$$I_d = I_o \exp(V_d/V_o) = I_o + I_b. \qquad \ldots(27)$$

All the relationships in the preceding sections can be used for bias conditions if I_o is replaced by I_d, and R_o by:

$$R = \frac{V_o}{I_o + I_b} = \frac{V_o}{I_d}.$$

The signal component at the output circuit should be separated from the bias current. The separation can be achieved by a.m. modulation of the microwave signal with a sinewave, and filtering the l.f. output signal to obtain the fundamental component. The sensitivity of the detector is defined in this case as the ratio of the r.m.s. value of the fundamental l.f. component to the total input power, which is dependent on the modulation depth. The a.m. modulated input voltage is:

$$V_i = (V_i)_{pk} (1 + a \cos pt) \cos \omega t, \qquad \ldots(28)$$

where a is the modulation depth and $p/2\pi$ the modulation frequency. The input power is then found to be:

$$P_i = \frac{\overline{V_i{}^2}}{R_i} = \frac{1}{2}\frac{(V_i)_{pk}{}^2}{R_i}(1 + \frac{1}{2}a^2). \qquad \ldots(29)$$

The fundamental component V_p of the output signal is proportional to the square of the barrier voltage:

$$\begin{aligned} V_{ac}{}^2 &= (V_{ac})_{pk}{}^2 (1 + a \cos pt)^2 \cos^2 \omega t \\ &= \frac{1}{2}(V_{ac})_{pk}{}^2 (1 + \frac{1}{2}a^2) + V_{ac}{}^2\, a \cos pt + \end{aligned} \qquad \ldots(30)$$

From Eq.5 the r.m.s. value of V_p becomes:

$$(V_p)_{rms} = \frac{\frac{1}{2}a\sqrt{2}}{2V_o}(V_{ac})_{pk}{}^2, \qquad \ldots(31a)$$

and:

$$(V_p)_{dc} = \frac{\frac{1}{2}(V_{ac})_{pk}{}^2}{2V_o} \ (a = 0). \qquad \ldots(31b)$$

Therefore:

$$\begin{aligned} (\beta_v)_p &= \frac{\frac{1}{2}a\sqrt{2}}{2V_o}(V_{ac})_{pk}{}^2 \frac{R_i}{\frac{1}{2}(V_i)_{pk}{}^2(1 + \frac{1}{2}a^2)}, \\ &= \frac{a\sqrt{2}}{1 + \frac{1}{2}a^2}\beta_v. \end{aligned} \qquad \ldots(32)$$

The voltage sensitivity (and also the current sensitivity) must be multiplied by the factor $a\sqrt{2}.\ [1 + \frac{1}{2}a^2]^{-1}$, when there is modulation. The factor becomes 0.94 for 100% modulation $(a = 1)$, and so approximately the same sensitivity can be reached as without modulation. From calculations it follows that the power sensitivity must be multiplied by a factor $2a^2\ [1 + \frac{1}{2}a^2]^{-1}$, and so the relevant factor becomes 4/3 for $a = 1$.

NOISE PERFORMANCE OF CRYSTAL DIODE

The noise performance of a crystal diode has been discussed by Torrey and Whitmer (Ref.1). To explain the origin of the noise in crystal diodes, the physics of the junction must be considered in greater detail. In this article, only the most important theorems and conclusions concerning the noise phenomena are given and discussed.

The diode has two noise sources. First, the spreading resistance r of the diode produces thermal (Johnson) noise, and second, the barrier produces 'shot' noise. The noise due to r is not considered here; the contribution of this noise source is in general small compared with that of the shot noise. Shot noise was investigated by Schottky, and he showed that the mean square noise current produced by a diode (under certain conditions) is given by:

$$\overline{i^2{}_n} = 2q_e I_d \Delta f, \qquad \ldots(33)$$

where q_e is the electronic charge, I_d the diode current, and Δf the bandwidth.

The current I_d flowing through the barrier is made up of two currents: $I_d = I_+ - 1_-$. The current I_+ is caused by the drift of the majority charge carriers because of the applied voltage V_d, and it has been shown that $I_+ = I_o \exp(V_d/V_o)$.

The current I_- is caused by diffusion due to the difference in concentration between the minority charge carriers at both sides of the barrier. This current is nearly independent of the applied voltage, and is found to be equal to the saturation current; that is, $I_- = I_o$. Consequently, the total current flowing through the diode becomes:

$$I_d = I_o \left\{\exp(V_d/V_o) - 1\right\}.$$

Therefore, at $V_d = 0$ where the two currents are balanced, the total current $I_d = 0$.

Both currents I_+ and I_- contribute to the noise level. These contributions are unrelated, and so the total noise current due to the barrier is given by:

$$\begin{aligned} \overline{(i^2{}_n)_t} &= 2\,q_e (I_+ + I_-)\,\Delta f, \\ &= 2\,q_e I_o \left\{\exp(V_d/V_o) + 1\right\} \Delta f. \end{aligned} \qquad \ldots(34)$$

Shot noise is independent of frequency (depending only on the bandwidth Δf), just like thermal noise caused by a resistance. The shot noise of the barrier can be expressed in terms of the noise temperature T_b of the barrier resistance R in such a way that:

$$\overline{(i^2{}_n)}_t = 4kT_bG\Delta f. \qquad \ldots(35)$$

with:

$$G = \frac{1}{R} = \frac{I_o}{V_o}\exp(V_d/V_o) = G_o\exp(V_d/V_o).$$

From Eqs.34 and 35 it can be shown that the noise temperature is:

$$T_b = \frac{1}{2}T\left\{1 + \exp(-V_d/V_o)\right\}, \ldots(36)$$

assuming $V_o = kT/q_e$.

At $V_d = 0$ the noise temperature T_b is equal to T; in other words the shot noise of the barrier then equals the Johnson noise due to the conductance G_o. When the voltage $V_d \gg V_o$, the noise temperature T_b is numerically nearly equal to half the ambient temperature T. This effect is not in contradiction with the second law of thermodynamics, because the barrier resistance R is not a ‘corporeal’ resistor but only a differential one.

The noise temperature T_b can be reduced by applying a bias current. At the working point $V = V_d$, the noise temperature T_b (from Eqs.27 and 36) is:

$$T_b = T\left\{\frac{1}{2} + \frac{I_o}{2(I_o + I_b)}\right\}. \qquad \ldots(37)$$

However, the bias current I_b introduces 1/f noise, and so the total noise temperature T_d of the diode becomes:

$$T_d = T\left\{\frac{1}{2} + \frac{I_o}{2(I_o + I_b)} + \frac{aI_b}{f}\right\}, \qquad \ldots(38)$$

in which the term a is a constant dependent on the kind of crystal diode. For the Schottky barrier diode the constant a is typically equal to 2Hz/μA, and for normal point-contact diodes equal to 3×10^4 Hz/μA.

Fig.7 shows a plot of noise temperature versus frequency with bias current as parameter.

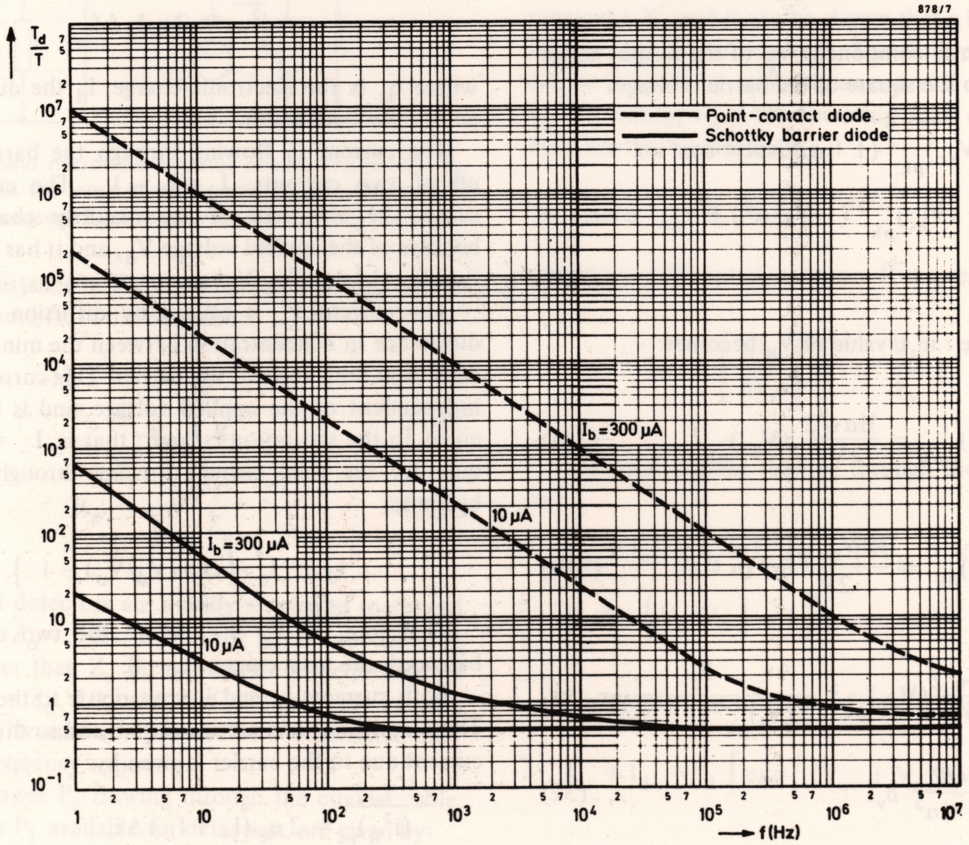

Fig.7 – Ratio between noise temperature T_d and ambient temperature T of a microwave diode as a function of frequency, with bias current I_b as parameter
Point-contact diode: I_o = 2.5μA, a = 3×10^4 Hz/μA
Schottky barrier diode: I_o = 2.5μA, a = 2Hz/μA

At the frequency given by:

$$f_f = 2aI_b \bigg/ \left(1 + \frac{I_o}{I_o + I_b}\right), \qquad \ldots(39)$$

the contribution of the 1/f noise equals the shot noise. To give a low noise level, the modulation frequency should exceed f_f.

NOISE EQUIVALENT POWER AND TANGENTIAL SENSITIVITY

At low level, the output power of a microwave detector is considerably lower than its input power because of the conversion loss. Consequently, the signal-to-noise ratio of the detector circuit is largely determined by the output circuit shown in Fig.8.

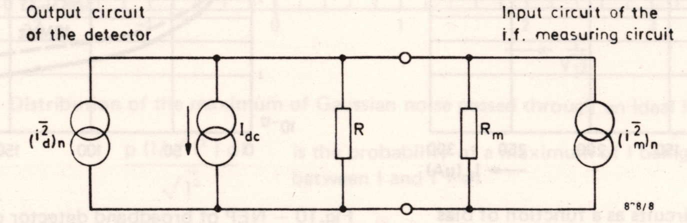
Output circuit of the detector
Input circuit of the i.f. measuring circuit
$\overline{(i^2{}_d)}_n$
I_{dc}
R
R_m
$\overline{(i^2{}_m)}_n$
8^78/8

Fig.8 – Output of the detector connected to the i.f. measuring circuit. Their noise sources are represented by $\overline{(i^2{}_d)}_n$ and $\overline{(^2{}_m)}_n$ respectively. R_m is the input resistance of the measuring circuit

The noise current $\overline{(i_d{}^2)}_n$ is governed by the barrier resistance R at the noise temperature T_d (defined in Eq.38). The equivalent noise source of the measuring system is denoted by $\overline{(i_m{}^2)}_n$. The total noise current is given by:

$$\overline{(i_t{}^2)}_n = \overline{(i_d{}^2)}_n + \overline{(i_m{}^2)}_n. \qquad \ldots(40)$$

With the noise factor given by:

$$F = \frac{\overline{(i_t{}^2)}_n}{\overline{(i_d{}^2)}_n} = 1 + \frac{\overline{(i_m{}^2)}_n}{\overline{(i_d{}^2)}_n},$$

the noise level becomes:

$$\overline{(i_t{}^2)}_n = F\,\overline{(i_d{}^2)}_n = 4kT_dFG\Delta f, \qquad \ldots(41)$$

where G = 1/R and Δf is the bandwidth determined by the measuring system. The signal-to-noise ratio becomes:

$$\frac{S}{N} = \frac{I_{dc}{}^2}{4kT_dFG\Delta f} = \frac{\beta_i{}^2P_i{}^2}{4kT_dFG\Delta f}, \qquad \ldots(42)$$

The a.c. power for which the signal-to-noise ratio is equal to unity is termed the noise equivalent power (NEP). It follows from Eq.42 that:

$$\begin{aligned} \text{NEP} &= \frac{\sqrt{(4kT_dFG\Delta f)}}{\beta_i}, \\ &= \frac{\sqrt{(4kT_dFR\Delta f)}}{\beta_v}, \\ &= \frac{\sqrt{(4kT_dF\Delta f)}}{\sqrt{(\beta_i\beta_v)}} \quad \text{W.} \end{aligned} \qquad \ldots(43)$$

The quantity $\sqrt{(\beta_i\beta_v)}$ is called the Figure of Merit M of the diode. However, a diode with an excellent Figure of Merit may have, nevertheless, a poor noise performance if the differential resistance has an extreme value so that the noise factor F is high.

The NEP can be reduced by applying a bias current, because the increase of the current sensitivity β_i, exceeds that of $\sqrt{G}$. However, at low modulation frequency the 1/f noise plays a role, and so the NEP can even be increased by applying a bias current. Figs.9 and 10 show the change of the NEP (at 10GHz) of several microwave detector circuits with various bias currents for different modulation frequencies applied. The NEP of tuned and broadband detector circuits, equipped with a point-contact diode as well as a Schottky barrier diode, is plotted in these figures. The noise factor F is assumed to be independent of the output impedance R, which varies with the bias current I_b, and the value of F has been taken as 2 for both types of diode. As expected, the NEP decreases by applying a bias current if a sufficiently high modulation frequency is used. The NEP of tuned detector circuits is minimum at a bias current of about 20 to 40μA. At a higher bias current the contribution of the 1/f noise becomes significant. This effect decreases with increasing modulation frequency.

Bias current reduces the NEP of a Schottky barrier diode considerably more than that of a point-contact diode because the I_o of the point-contact diode is 10^3 times that of the Schottky barrier diode.

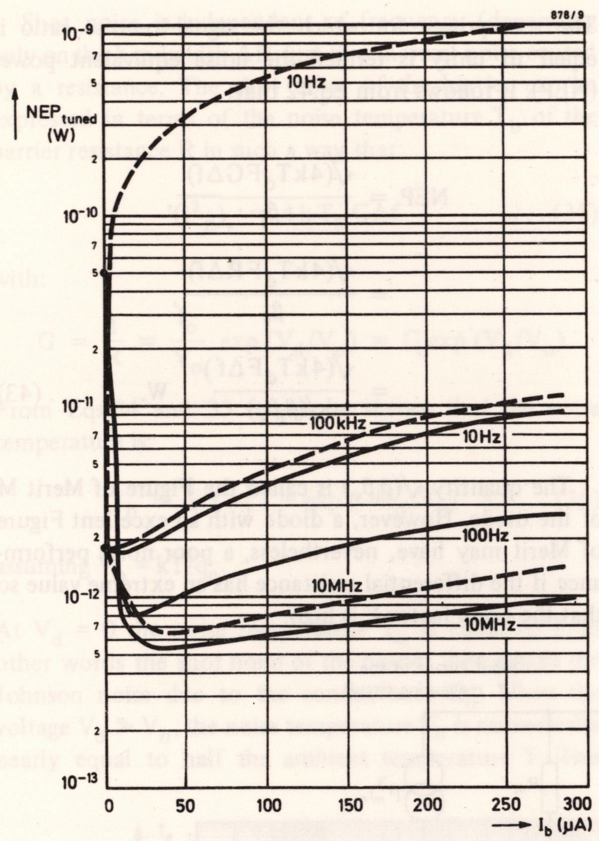

Fig.9 – NEP of tuned detector circuits as a function of bias current with modulation frequency as parameter.
Broken line point-contact diode with:
$I_o = 2.5 \times 10^{-6}$ A,
V_o = 25mV,
r = 10Ω, C = 0.28pF,
a = 3×10^4 Hz/μA
Continuous line Schottky barrier diode with:
$I_o = 2.5 \times 10^{-9}$ A,
V_o = 25mV,
r = 10Ω, C = 0.2pF,
a = 2Hz/μA

Finally, as expected, the NEP of broadband detectors exceeds that of tuned detectors under the same conditions.

Tangential Sensitivity
The tangential sensitivity (TSS) of a detector circuit is often given instead of the NEP. The TSS can be explained using the block diagram shown in Fig.11. The generator power is switched on and off in the periods A and B respectively. The output of the detector is amplified and shown on an oscilloscope. The difference in the mean values of the level during the periods A and B is proportional to the a.c. input power. The TSS is defined with the help of two levels indicated by the lines a and b.

The noise signal during A exceeds level a for 90% of the time, and the noise signal during B exceeds level b for 10% of the time, The TSS is the input power at which a and b are in a straight line.

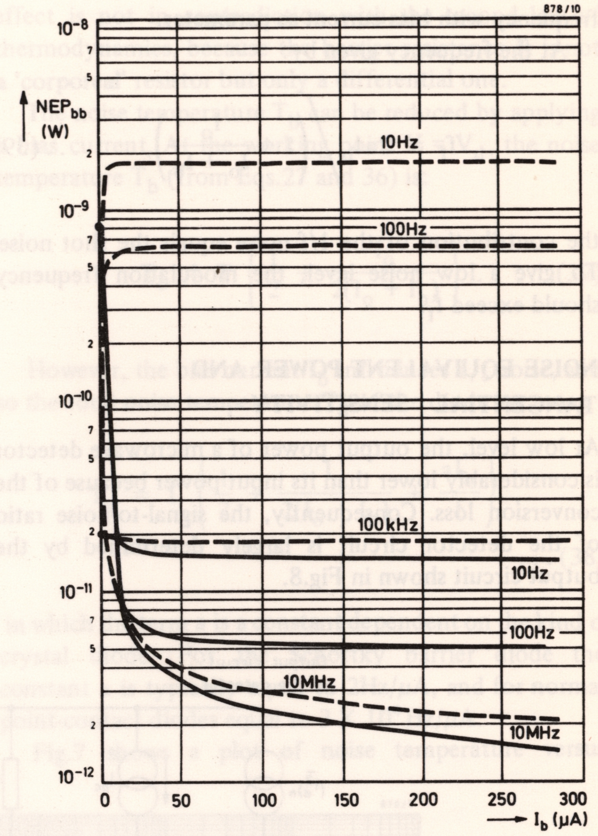

Fig.10 – NEP of broadband detector circuits as a function of bias current with modulation frequency as parameter:
broken line point-contact diode
continuous line Schottky barrier diode
(For data, see Fig.9)

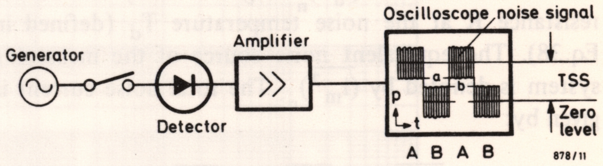

Fig.11 – Measurement of tangential sensitivity TSS of a detector circuit

Rice calculated the distribution of Gaussian noise passed through an ideal lowpass filter (Ref.5). This distribution is shown in Fig.12. The '10% line' corresponds to a level which is equal to 2.5 times the r.m.s. value of the noise signal, where TSS = 5 × NEP.

SOME MEASUREMENTS ON POINT-CONTACT DIODES

The low-level detection properties of a microwave diode have been derived above from its d.c. characteristic and its barrier capacitance; in this calculation an idealised equivalent circuit has been used, and the parasitic impedances of the cartridge have been left out of account. Now the question arises as to how closely the theoretical values agree with the actual ones. In order to investigate this, the 'I V' characteristic of some typical diodes has been measured to obtain the voltage V_o and the spreading resistance r. In addition, the differential resistance R_o and the barrier capacitance C have been measured at 1MHz. Finally, the various kinds of sensitivity of the diodes have been measured at 10GHz. Before the discussion of the results, listed in Table 2, a short description of the measuring methods used is given.

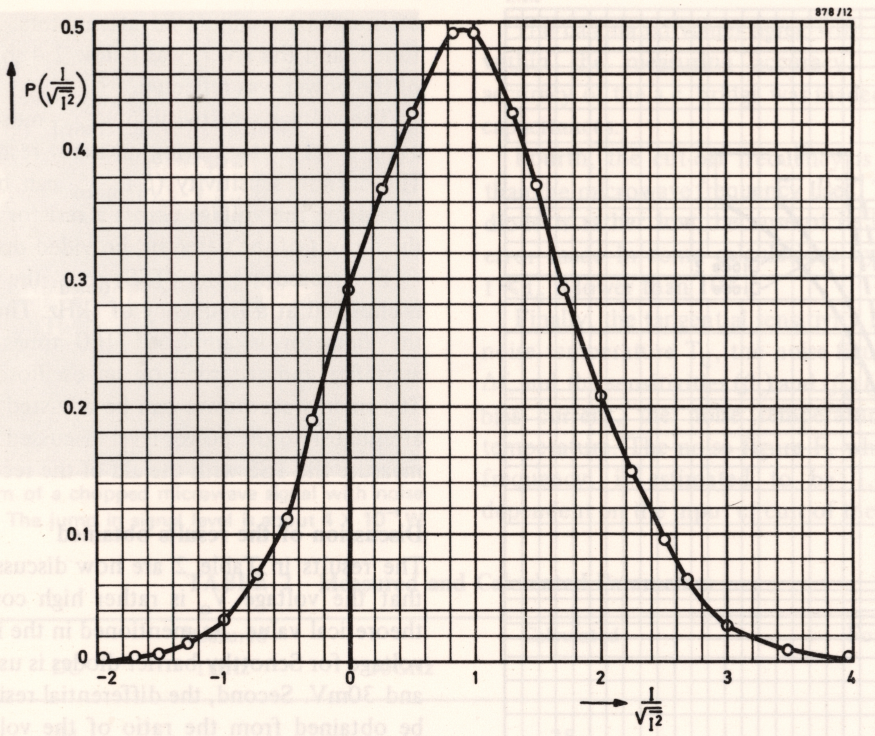

Fig.12 – Distribution of the maximum of Gaussian noise passed through an ideal low-pass filter

$\frac{p(I/\sqrt{\overline{I^2}})\,dI}{\sqrt{\overline{I^2}}}$ is the probability of a maximum of I being between I and I + dI

Measuring 'I V' characteristics
The 'I V' characteristic of the diode can be measured using normal high-impedance millivoltmeters or a curve tracer, as shown in Fig.13.

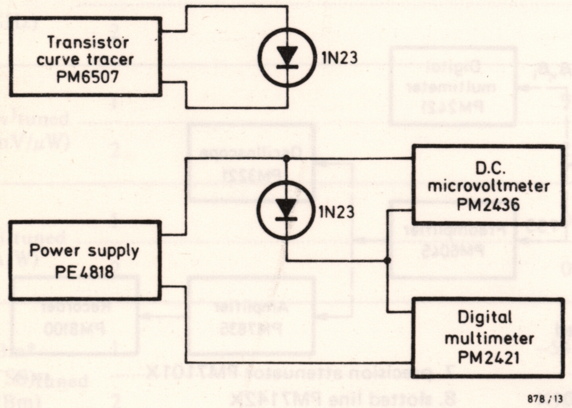
Transistor curve tracer PM6507
1N23
Power supply PE4818
1N23
D.C. microvoltmeter PM2436
Digital multimeter PM2421
878/13

Fig.13 – Block diagrams of ways of measuring 'IV' characteristic

The characteristic has been measured up to 10mA; a higher current might damage the diode. In Fig.14 the currents of two diodes are plotted on a logarithmic scale as a function of voltage. The straight part of the curve corresponds to the voltage range $V \gg V_o$ (where the voltage drop over r is negligibly small), and we obtain $I = I_o \exp(V/V_o)$ to a first approximation.

The voltage V_o can be found from the two points (V_1, I_1) and (V_2, I_2) on that part of the curve, and we find that:

$$V_o = \frac{V_2 - V_1}{\log_e (I_2/I_1)} \,. \qquad \ldots (44)$$

The series resistance r can be obtained from the deviation of the characteristic from the straight line (see Fig.14).

Measuring R_o and C with a bridge at 1MHz
The differential resistance R_o and the barrier capacitance C can be measured by using an a.c. bridge at 1MHz. R_o can also be obtained from the 'I V' characteristic, but the bridge method turns out to be more accurate. As we are only interested in the capacitance of the barrier, the capacitance of the cartridge must be compensated. For this purpose the bridge is balanced with the cartridge alone. After balancing, the diodes were measured. It

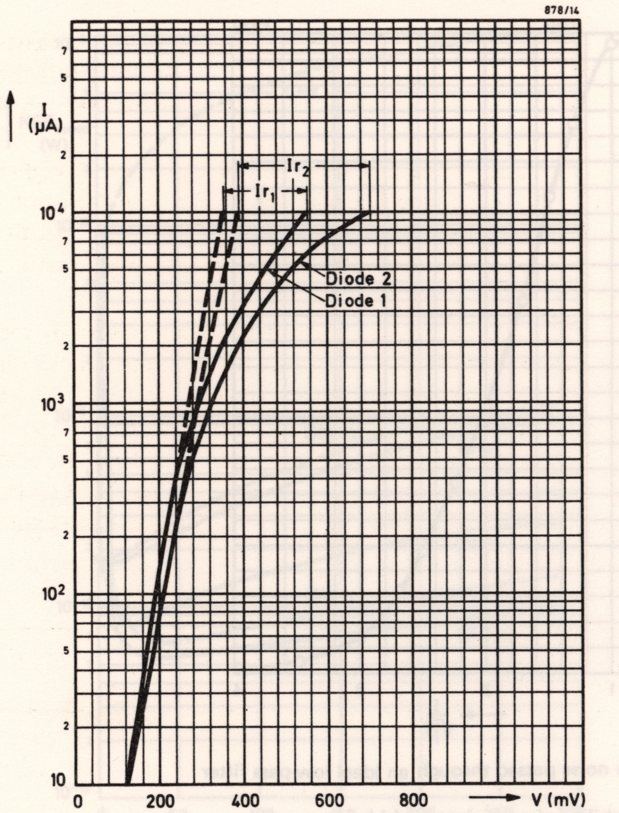

Fig.14 – 'IV' characteristics of two point-contact diodes. The series resistance r can be obtained from the deviation from the straight line

should be noted that the level of the measuring signal was below 5mV in order to avoid difficulties arising from the non-linearity of the characteristic of the diode.

Measuring $(\beta_v)_{tuned}$, $(\beta_i)_{tuned}$, and $(TSS)_{tuned}$ at 10GHz

The sensitivities $(\beta_v)_{tuned}$, $(\beta_i)_{tuned}$, and $(TSS)_{tuned}$ were measured at 10GHz with the measuring arrangement shown in Fig.15.

The microwave power, measured by a tuned thermistor, was adjusted at a level of 1mW. This power is attenuated by calibrated attenuators. The detector was tuned, and the s.w.r. was below 1.4 so that less than 3% of the power was reflected.

The voltage sensitivity $(\beta_v)_{tuned}$ must be measured by using a voltmeter having an input resistance $R_m \gg R_o$. The current sensitivity $(\beta_i)_{tuned}$ can be determined by measuring the voltage across a resistor R_k connected to the output of the detector, provided that $R_k \ll R_o$.

For measuring the $(TSS)_{tuned}$, the microwave signal is chopped at a frequency of 1kHz. The output signal of the detector is amplified 100 times by a low-noise amplifier and recorded on an oscilloscope (see Fig.16). The microwave power can be adjusted by the calibrated attenuator to the power level discussed above in order to measure the TSS with the aid of the recorder PM8100.

Discussion of the results obtained

The results in Table 2 are now discussed. First, we see that the voltage V_o is rather high compared with the theoretical value. As mentioned in the introduction, this voltage for Schottky barrier diodes is usually between 26 and 30mV. Second, the differential resistance R can also be obtained from the ratio of the voltage and current sensitivites. From the values in Table 2 we get $(R_o)_1$ = 49kΩ and $(R_o)_2$ = 27kΩ.

Third, the sensitivity of the detector circuit is nearly inversely proportional to the barrier capacitance (see Eqs.18 and 19), and so we obtain:

$$C_1 = \frac{1}{\sqrt{\{2\omega^2 r V_o (\beta_v)_{tuned}\}}} =$$

$$= \frac{1}{\sqrt{(2 \times 4 \times \pi^2 \times 10^{20} \times 24 \times 34 \times 10^{-3} \times 9.4 \times 10^3)}},$$

$$= 0.13\text{pF};$$

$$C_2 = \frac{1}{\sqrt{(2 \times 4 \times \pi^2 \times 10^{20} \times 34 \times 38 \times 10^{-3} \times 2.7 \times 10^3)}},$$

$$= 0.19\text{pF}.$$

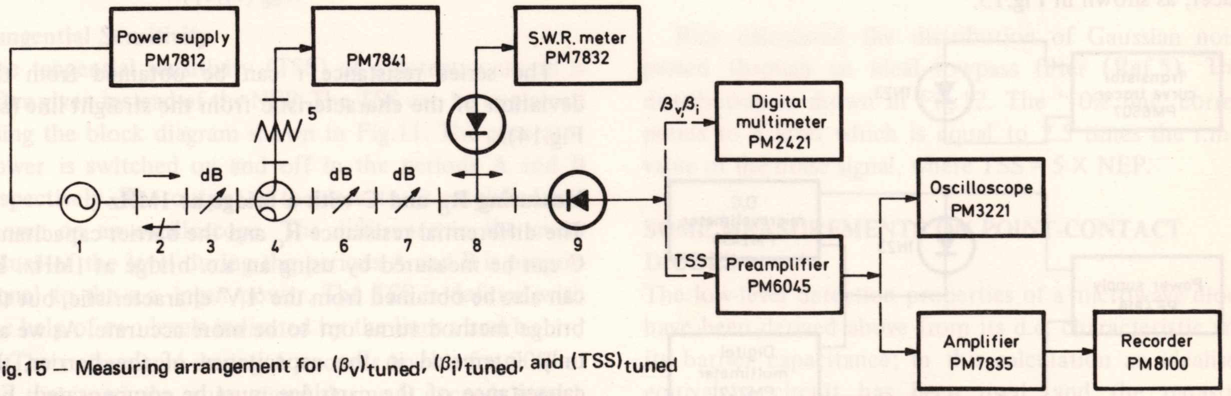

Fig.15 – Measuring arrangement for $(\beta_v)_{tuned}$, $(\beta_i)_{tuned}$, and $(TSS)_{tuned}$

1. oscillator PM7011X
2. isolator PM7045X
3. level attenuator PM7110X
4. switch PM7305X
5. thermistor head PM7201X
6. precision attenuator PM7101X
7. precision attenuator PM7101X
8. slotted line PM7142X
9. tunable detector PM7185X

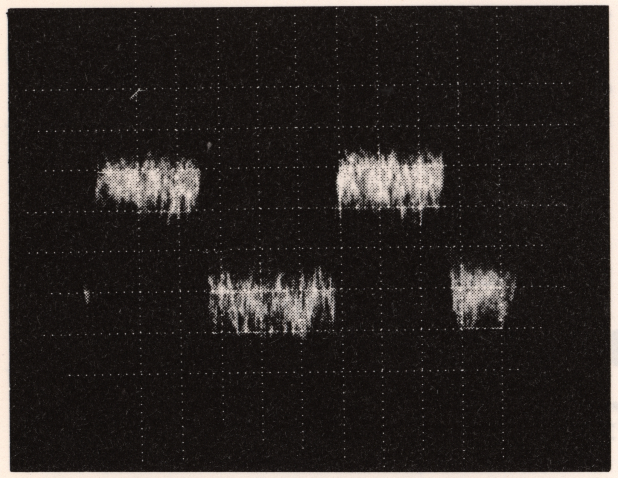

Fig.16 – Oscillogram of a chopped microwave signal with noise for measuring TSS. The jump in signal level is about 4×10^{-9} W

The calculated values agree with the measured values within the measuring accuracy. Unfortunately, the accuracy of the a.c. bridge was inadequate for these small capacitances.

Fourth, the cut-off frequency is significantly higher than the microwave frequency used. The f_c of the second diode is rather low, because of its high r; however, the error made in some calculations by the approximation $f \ll f_c$ is lower than 10%.

Finally, the tangential sensitivity is determined by the noise temperature T_d, the noise figure F, the bandwidth Δf, and the sensitivities (β_v) and (β_i) (see Eq.43). Without bias current, the noise temperature T_d equals room temperature. The noise figure F, which is dependent on frequency, is estimated to be 1.6. The bandwidth, dependent on the input circuit of the amplifier, is estima-

TABLE 2 Measured and Calculated Parameters

		Measured			Calculated	Formulae
		DC	1MHz	10GHz		
V_o (mV)	1	34			25	$V_o = \frac{4kT}{q_e}$
	2	38			25	
r (Ω)	1	24				
	2	34				
R_o (kΩ)	1		50.4		49	$R_o = \frac{(\beta_v)_{tuned}}{(\beta_i)_{tuned}}$
	2		31.4		27	
C (pF)	1		0.1–0.2		0.13	$C = \frac{1}{\sqrt{\{2\omega^2 r V_o (\beta_v)_{tuned}\}}}$
	2		0.15–0.25		0.19	
I_o (μA)	1				0.7	$I_o = \frac{V_o}{R_o}$
	2				1.2	
f_e (GHz)	1				51	$f_c = \frac{1}{2\pi rC}$
	2				25	
$(\beta_v)_{tuned}$ (mV/μW)	1			9.4		
	2			2.7		
$(\beta_i)_{tuned}$ (A/W)	1			0.19		
	2			0.1		
dBm* $(TSS)_{tuned}$ (dBm)	1			−54	−52.6	$(TSS)_{tuned} = 5 \left[\frac{4kT_dF\Delta f}{(\beta_v)_{tuned}(\beta_i)_{tuned}}\right]^{1/2}$
	2			−50	−48.5	

*O dBm = 1mW

ted to be 80kHz. The sensitivities $(\beta_v)_{\text{tuned}}$ and $(\beta_i)_{\text{tuned}}$ are taken from Table 2, and we have:

$$(\text{TSS})_1 = 5 \left[\frac{4\text{kF}\Delta\text{f}}{\beta_i \beta_v} \right]^{\frac{1}{2}} =$$

$$= 5 \left[\frac{4 \times 1.4 \times 10^{-23} \times 300 \times 1.6 \times 8 \times 10^4}{9.4 \times 10^3 \times 1.9 \times 10^{-1}} \right]^{\frac{1}{2}} =$$

$$= 5.5 \times 10^{-9} = 52.6\text{dBm};$$

and:

$$(\text{TSS})_2 = 5 \left[\frac{4 \times 1.4 \times 10^{-23} \times 300 \times 1.6 \times 8 \times 10^4}{2.7 \times 10^3 \times 10^{-1}} \right]^{\frac{1}{2}} =$$

$$= 14 \times 10^{-9} = 48.5\text{dBm}.$$

These values agree very well with the measured values.

We can therefore conclude that the simplified model of the detector can be used for calculating the sensitivity and TSS of the detectors at least to a first approximation.

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Mains-operated switched-mode power supply for an oscilloscope

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Mullard Application Laboratory

A switched-mode power supply is described which provides five outputs at 180V, 18V, 6.3V, −18V, and −2kV, with a total output power of 18W. The output voltage regulation is better than 1% and the efficiency is greater than 70%. The measured radio frequency interference from the laboratory prototype power supply is approximately in accordance with the VDE 0875 'K' specification, and well below the BS 800 and VDE 0875 'N' specifications.

INTRODUCTION

The laboratory prototype switched-mode power supply described in this article was constructed both to demonstrate the performance of a flyback converter when used in an oscilloscope power supply, and to investigate some of the design problems arising, particularly in the transformer. Construction details are given, together with performance figures, and special attention is paid to the reduction of radio frequency interference (see Ref.1) without the use of interference screens in the transformer.

DESIGN SPECIFICATION

The laboratory prototype oscilloscope power supply was designed to meet the following specification, which is typical for a small oscilloscope.

Input	220V + 10% − 15%, at 50Hz or 60Hz
Outputs (referred to common line except where stated)	1) −2kV, 100 to 500μA with a variable load; maximum ripple = 1V peak-to-peak 2) +180V, 70mA with a fixed load; maximum ripple = 0.5V peak-to-peak 3) +18V, 100mA with a fixed load; maximum ripple = 10mV peak-to-peak 4) −18V, 100mA with a fixed load; maximum ripple = 10mV peak-to-peak 5) 6.3V, 750mW referred to −2kV line; c.r.t. heater supply
Output regulation	2% voltage regulation against supply voltage and 2kV load changes
Total output power	18W

CIRCUIT DESCRIPTION

The complete circuit diagram for the oscilloscope power supply is shown in Fig.1. The mains supply is connected to bridge rectifier D_{13} and reservoir capacitor C_{14} via interference filters, which have a surge-limiting series resistance of 3.6Ω. The d.c.-to-d.c. converter is of the flyback type (Ref.2). In operation, the rectified mains voltage is applied to the primary of transformer T_1 while the power-switching transistor TR_5 is switched on, and energy is stored in the transformer. When TR_5 is switched off, the voltages on the transformer windings change polarity, and the stored energy is supplied to the loads via the isolated secondary windings. Two additional

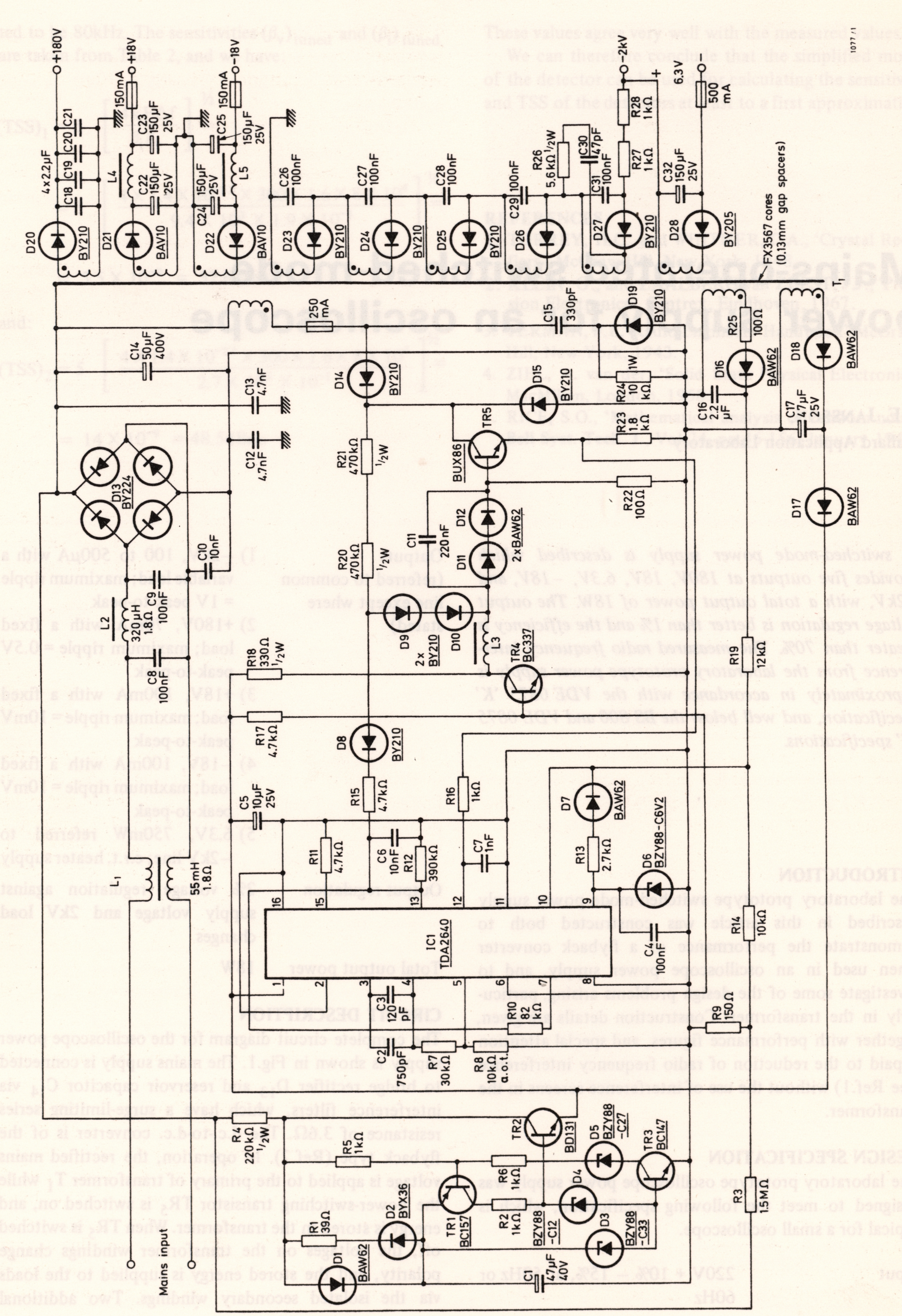

+180V
+18V
–18V
150mA
150mA
4×2.2µF
C18
C19
C20
C21
L4
C22 150µF 25V
C23 150µF 25V
C24 150µF 25V
C25 150µF 25V
L5
D20 BY210
D21 BAV10
D22 BAV10
C26 100nF
D23 BY210
C27 100nF
D24 BY210
C28 100nF
D25 BY210
C29 100nF
D26 BY210
R26 5.6kΩ ½W
C30 47pF
C31 100nF
–2kV
R28 1kΩ
R27 1kΩ
D27 BY210
6.3V
500mA
C32 150µF 25V
D28 BY205
FX3567 cores (0.13mm gap spacers)
T1
250mA
C14 50µF 400V
C13 4.7nF
C12 4.7nF
D13 BY224
C10 10nF
D14 BY210
R21 470kΩ ½W
R20 470kΩ ½W
C15 330pF
D19 BY210
R25 100Ω
D18 BAW62
D15 BY210
R24 10kΩ 1W
D16 BAW62
C16 2.2µF
C17 47µF 25V
TR5 BUX86
R23 1.8kΩ
R22 100Ω
D17 BAW62
D12
D11
2×BAW62
C11 220nF
L2 320µH 1.8Ω
C9 100nF
D9
D10
2× BY210
L3
TR4 BC337
R19 12kΩ
R18 330Ω ½W
C8 100nF
R17 4.7kΩ
D8 BY210
R15 4.7kΩ
R16 1kΩ
D7 BAW62
C5 10µF 25V
C6 10nF
R12 390kΩ
C7 1nF
R13 2.7kΩ
D6 BZY88-C6V2
R14 10kΩ
L1 55mH 1.8Ω
R11 4.7kΩ
IC1 TDA2640
C3 120pF
C4 100nF
R10 82kΩ
R9 150Ω
C2 750pF
R8 10kΩ a.o.t.
R7 30kΩ
R4 220kΩ ½W
R5 1kΩ
TR2 BD131
D5 BZY88 –C27
TR3 BC147
R6 1kΩ
R3 1.5MΩ
D2 BYX36
R1 39Ω
Mains input
D1 BAW62
TR1 BC157
R2 1kΩ
D4 BZY88 –C12
D3 BZY88 –C33
C1 47µF 40V

Fig.1 – Circuit diagram of oscilloscope power supply

secondary windings, each providing 13V, are used to supply the TDA2640 control IC, IC_1, and to apply voltage control feedback.

The TDA2640 IC (Ref.3) is used for waveform generation, voltage control, and overcurrent protection. The output voltage is regulated by varying the duty factor of TR_5, under the control of feedback (to pin 10) from one of the 13V auxiliary windings. The second auxiliary winding provides the positive supply voltage for the IC during normal operation, but at switch-on, when the supply voltage on pin 1 is initially zero, the start circuit at the left-hand side of Fig.1 comes into operation. Capacitor C_1 discharges via TR_2 to provide a 12V supply for 20ms to start the circuit.

Base drive for TR_5 is controlled by TR_4, which inverts and amplifies the rectangular output waveform of the TDA2640. The inductor L_3 controls the base-charge extraction of TR_5 to minimise its turn-off dissipation (see Ref.4).

The collector voltage of TR_5 (via R_{20} and R_{21}) is gated by the base drive waveform (via D_9 and D_{10}), to monitor the collector voltage during the base drive time. If the collector voltage of TR_5 starts to rise, the voltage on pin 13 of the TDA2640 also rises; this reduces the duty factor and avoids undesirable saturation of the transformer during the initial charging period of the output smoothing capacitors.

To supplement the overcurrent protection provided by the TDA2640, diodes D_{14} and D_{15} are included. These prevent oscillation in TR_5, when the power supply outputs are short-circuited and the collector load of TR_5 consists mainly of transformer leakage inductance. Current limiting resistors R_{27} and R_{28} prevent damage to diodes D_{23} to D_{27} by back e.m.f. across the wiring inductance, which could result from excessive discharge current from the –2kV output. Diodes D_{21}, D_{22}, and D_{28}, which supply the three low-voltage outputs, are protected by fuses as shown in Fig.1.

The feedforward connection via R_3 is included to minimise 100Hz ripple on the outputs.

TRANSFORMER DESIGN

The design of the transformer in a flyback converter is particularly important because it dictates the voltage and current waveforms of the power-switching transistor. This section describes the theoretical calculations which were made before construction.

Maximum flyback voltage

In flyback converters in which the power-switching transistor is switched on while stored energy remains in the transformer, the first constraint on transformer design is the maximum collector voltage permitted by the transistor safe operating area data when the transistor is on. For the BUX86 this voltage is 700V, and with a 220V +10% mains supply the maximum rectified voltage is 340V. Therefore, the maximum permissible flyback voltage on the transformer primary is (700 – 340) = 360V.

As the output voltage required by the major load is 180V, this leads to a 2:1 turns ratio, which simplifies the transformer winding design. It should be noted, however, that this 2:1 ratio allows no safety factor for maladjustment of the output voltage, which could increase the flyback voltage V_{op}. For operation on 240V mains, the maximum flyback voltage should be reduced, to 300V for example.

The theoretical transformer voltage, flux, and current waveforms with V_{op} = 360V are shown in Fig.2 for two operating conditions; Fig.2a shows the waveforms for a d.c. supply voltage V_{ip} of 360V, and Fig.2b shows the waveforms for a V_{ip} of 180V. The duty cycle for each of these conditions can be calculated from:

$$V_{ip} \cdot \delta = V_{op}(1 - \delta), \qquad \ldots (1)$$

where V_{op} and V_{ip} have already been defined, and δ is the duty factor (the ratio of the switching transistor on-time to the total cycle time). From this equation, δ in Fig.2a is ½, and δ in Fig.2b is 2/3.

Volts per turn

A basic expression for transformer operation is:

$$V = N\frac{d\Phi}{dt}, \qquad \ldots (2)$$

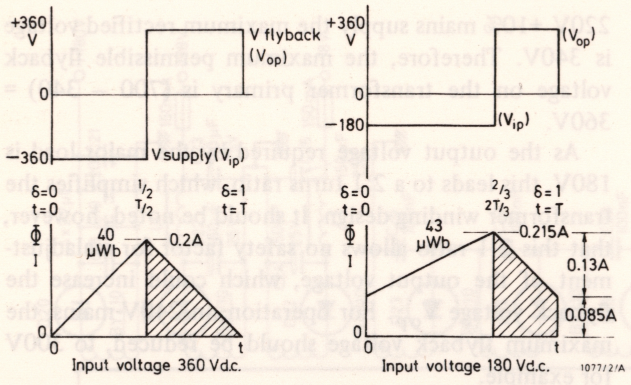
where V is the voltage developed across N turns when the flux changes by an amount dΦ in time dt. As shown in Fig.2a, where the duty factor δ is ½, the flux changes from its peak value Φ_{pk} to zero in a time T/2, where T is the total cycle time. The volts per turn in the flyback period (and also during the transistor conduction period when V_{ip} = 360V) is therefore given by:

$$\frac{V}{N} = \frac{2\Phi_{pk}}{T}, \qquad \ldots (3)$$

$$= 2\Phi_{pk} f, \qquad \ldots (4)$$

where f is the operating frequency.

It can be seen that the number of turns on the high-voltage windings can be minimised only by using a large peak flux and a high operating frequency. A frequency of 33kHz was chosen to give an acceptable compromise between transformer design problems and transistor switching losses. To obtain a high peak flux, a pair of FX3567 ferrite cores were chosen which have, within a maximum dimension of 44mm, a large circular centre pole area of about 200mm². The saturation flux density of these cores is in excess of 340mT at 85°C, and to avoid saturation and to limit core losses, the peak flux density



(a) (b)

Fig.2 – Transformer voltage, flux, and current waveforms, all referred to the primary

was chosen to be 200mT. The core loss with a bidirectional magnetisation of 200mT at 33kHz would be approximately twice the published 16kHz figure of <2W, giving <4W, and with unidirectional magnetisation an acceptable loss of about 1W could be expected.

The peak flux is given by:

$$\Phi_{pk} = \text{peak flux density} \times \text{centre pole area},$$

$$= 200 \times 10^{-3} \times 200 \times 10^{-6}\ \text{Wb},$$

$$= 40\mu\text{Wb}.$$

Using this value of Φ_{pk}, the volts per turn during the flyback period is given from Eq.4 by:

$$\frac{V}{N} = 2 \times 40 \times 10^{-6} \times 33 \times 10^3,$$

$$= 2.6\text{V}.$$

In the practical transformer, this was reduced to 2.4V per turn to obtain whole numbers of turns on the low-voltage windings.

Primary inductance

To provide an output power of 18W, the required current with a 360V d.c. input is given by:

$$I = \frac{18}{360},$$

$$= 0.05\text{A d.c.}$$

This average current is an average over the total cycle time T, but is supplied to the output only during the flyback time $(1 - \delta)$T. With the triangular waveform shown in Fig.2a the duty cycle δ = ½, so the average current supplied over the flyback period must be 2 × 0.05 = 0.1A; and as the waveform during the flyback period is triangular, the peak current is twice the average. The peak current is therefore 0.2A, as shown in Fig.2a.

From the basic expression:

$$V = L\frac{dI}{dt}, \qquad \ldots (5)$$

the inductance L_p of the primary is given by:

$$L_p = V_{op}\frac{\Delta t}{\Delta I}, \qquad \ldots (6)$$

where Δt is the duration of the flyback period and ΔI is the change of current during this period. For a d.c. supply of 360V, Δt = T/2 and ΔI = 0.2A as calculated above. Using the value of 360V for V_{op}:

$$L_p = 360 \times \frac{1}{0.2 \times 2 \times 33 \times 10^3}\ \text{H},$$

$$= 27\text{mH}.$$

This inductance is obtained in practice by the use of an appropriate transformer gap spacing.

Operation on low supply voltage

From Eq.6, the change in current during the flyback period is given by:

$$\Delta I = \frac{V_{op}}{Lp} \cdot \Delta t. \qquad \ldots (7)$$

Substituting for Δt in terms of T and δ:

$$\Delta I = \frac{V_{op}}{Lp}(1 - \delta)T. \qquad \ldots (8)$$

If the d.c. supply voltage is reduced to 180V, δ changes to 2/3, and the change in current is given by:

$$\Delta I = \frac{360}{27 \times 10^{-3}} \times \left(1 - \frac{2}{3}\right) \times \frac{1}{33 \times 10^3},$$

$$= 0.13\text{A}.$$

Referring to Fig.2b, this value is the height of the triangular part of the current waveform during flyback. The average value of this triangular part is half the height; that is, 0.065A.

To supply the required average current over time T, that is 0.05A, the average current during the flyback period (= T/3) must be 3 × 0.05 = 0.15A.

The height of the 'pedestal' of the current waveform in the flyback period is given by the difference between the total average current and the average of the triangular part. Therefore:

$$\text{pedestal height} = 0.15 - 0.065, \quad = 0.085\text{A}.$$

The peak current during the flyback period for a 180V supply is therefore 0.085 + 0.13 = 0.215A, and the peak flux also increases, compared to the value of 40μWb for a 360V supply, in the ratio 0.2:0.215; the new value is 43μWb.

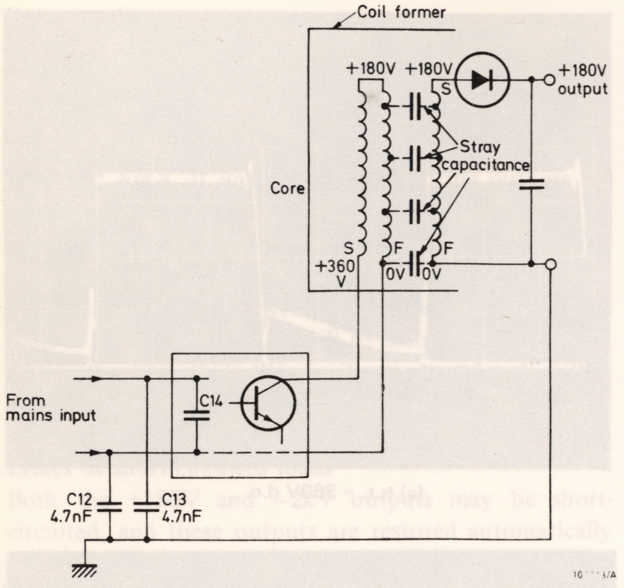


Fig.3 – Winding configuration requiring no r.f.i. screen; component numbers refer to Fig.1

From the figures calculated above, the peak flux and peak collector current increase by only 7.5% when the d.c. supply voltage is reduced from 360V to 180V.

Design of windings to minimise radio frequency interference (r.f.i.)

The use of r.f.i. screening in a transformer increases the capacitance in the transformer, and results in an increase in the power-switching transistor current spike at turn-on. To avoid this problem, the method of reducing r.f.i. without screening shown in Fig.3 was employed. As the primary voltage during flyback was chosen to be twice that of the major +180V output, the primary occupies two winding layers and the secondary one layer, if the same gauge wire is used for both windings. Hence, with the winding directions and connections shown in Fig.3, there is no potential difference between adjacent primary and secondary turns throughout the windings. Generation of an interference voltage between the mains input terminals and earth by current flowing through the primary to secondary stray capacitance is therefore avoided.

CONSTRUCTION OF THE PROTOTYPE TRANSFORMER

The layout of the windings, the wire gauges, and the interlayer insulation employed are illustrated in Fig.4. The starts of all windings are located on the same (left-hand) side of the former to improve the accuracy of alignment of the windings on top of each other. Another advantage of starting both layers of the primary on the same side of the former is that this reduces the effective self-capacitance of the winding to one quarter of the total layer-to-layer capacitance, whereas the effective self-capacitance for the configuration illustrated in Fig.3 is one-third of the total layer-to-layer capacitance. Hence the arrangement shown in Fig.4 gives the minimum effective self-capacitance for the insulation thickness employed, and this insulation thickness must be kept as small as possible to minimise the leakage inductance between the primary and the 180V secondary which supplies the major part of the output power. A low value of leakage inductance is necessary to minimise the overshoot on the collector voltage when the power-switching transistor is turned off.

The design of the high-voltage windings is governed by three factors: the volts per turn, which has already been fixed at the highest practicable value; the contribution of the secondary to the total stray capacitance in the transformer; and the minimum wire size which can be easily handled and economically wound in production. Using 0.08mm diameter wire as the minimum, five layers of wire are required to produce 2kV. In a continuous winding of five layers, however, the interlayer capacitance would produce very large current spikes and unacceptable ringing.

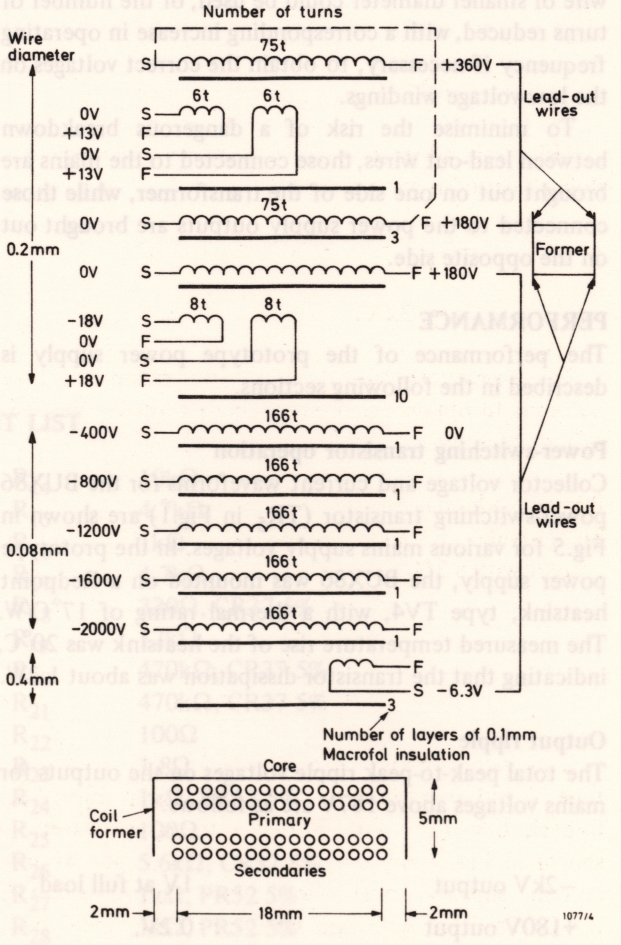


Fig.4 – Transformer construction details

The secondary winding for the −2kV output is therefore split into five 400V sections, each with its own rectifier diode and smoothing capacitor (see Fig.1). The low-potential ends of these five windings are joined by the smoothing capacitors, and the high-potential ends have identical voltage excursions, so that no voltage changes occur across the interlayer capacitance of the secondary to contribute to current spikes. The only contribution to current spikes comes from the first 400V winding, and to limit this contribution to a value similar to that produced by the primary, the insulation thickness between the first winding and the previous windings is adjusted to take account of the high effective voltage difference between these layers. As the low-voltage secondary windings are located at the low-potential ends of the high-voltage windings, their contribution to current spikes can be ignored.

As illustrated in Fig.4, the windings occupy a width of 18mm, with a 2mm gap between each end of the windings and the former. This gives a creepage distance of 4mm between the primary and the secondary. To meet the strictest safety isolation specifications, especially with unimpregnated transformers, it may be necessary to increase the creepage distance to 8mm. To achieve this, wire of smaller diameter could be used, or the number of turns reduced, with a corresponding increase in operating frequency if necessary, to obtain the correct voltages on the low-voltage windings.

To minimise the risk of a dangerous breakdown between lead-out wires, those connected to the mains are brought out on one side of the transformer, while those connected to the power supply outputs are brought out on the opposite side.

PERFORMANCE

The performance of the prototype power supply is described in the following sections.

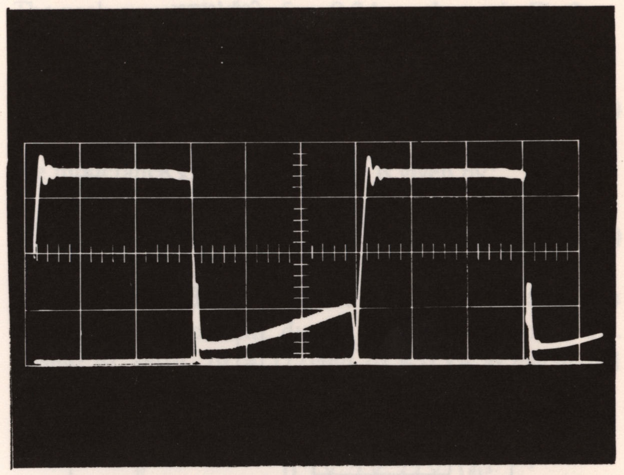
Power-switching transistor operation

Collector voltage and current waveforms for the BUX86 power-switching transistor (TR_5 in Fig.1) are shown in Fig.5 for various mains supply voltages. In the prototype power supply, the BUX86 was mounted on a Redpoint heatsink, type TV4, with a thermal rating of 17°C/W. The measured temperature rise of the heatsink was 20°C, indicating that the transistor dissipation was about 1.2W.

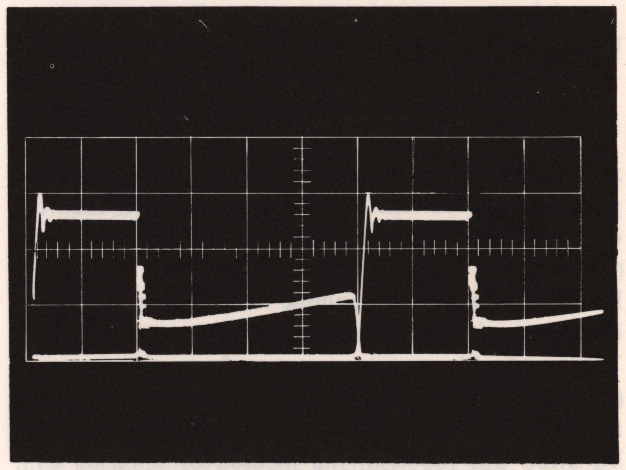
Output ripple

The total peak-to-peak ripple voltages on the outputs for mains voltages above 187V are as follows:

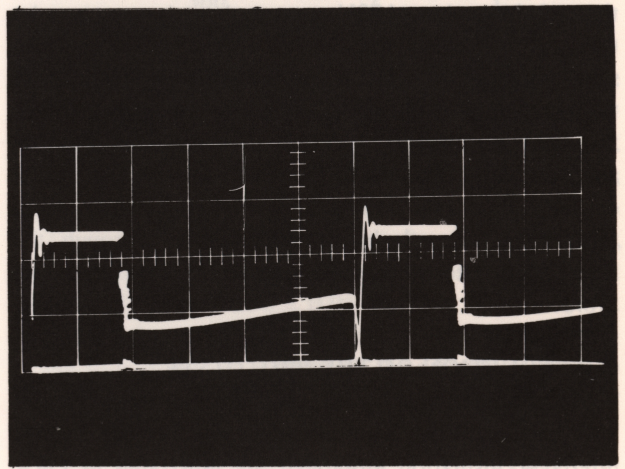
−2kV output	1V at full load,
+180V output	0.2V,
+18V and −18V outputs	10mV.



(a) h.t. = 360V d.c.



(b) h.t. = 180V d.c.



(c) h.t. = 140V d.c.

Fig.5 – Power-switching transistor collector voltage and current waveforms

Vertical scales: 200V/div
0.2A/div
Horizontal scale: 5µs/div

Output voltage regulation

The variation of output voltages with mains voltage is shown in Fig.6, the output regulation of the 180V 70mA output against load is shown in Fig.7, and that of the −2kV output over its load range of 100 to 500µA is shown in Fig.8. It will be seen that all the outputs are stable to within about 1% for line and load variations.

Radio frequency interference

The measured r.f.i. between the mains input and earth leads is shown in Fig.9. It will be seen that it is largely within the VDE 0875 'K' specification, and well within the BS 800 and VDE 0875 'N' specifications.

Effect of short-circuited loads

Both the +180V and −2kV outputs may be short-circuited, and these outputs are restored automatically when the short-circuit is removed. Fuses are employed (as shown in Fig.1) to protect the output diodes which supply the +18V, −18V, and 6.3V outputs.

Efficiency

The overall efficiency, measured from a.c. mains input to total d.c. output, is 74% with a 220V mains supply, and remains within 2% of this figure over the mains voltage range of +10% to −15%.

REFERENCES

1. JANSSON, L.E., 'Radio frequency interference suppression in switched-mode power supplies', Technical Note 30, TP1443/1, Mullard Limited, 1975.
2. JANSSON, L.E., 'A survey of converter circuits for switched-mode power supplies', Technical Note 24, TP1442/1, Mullard Limited, 1975.
3. 'TDA2640 control IC for switched-mode power supplies', Technical Information 19, TP1509, Mullard Limited, 1975.
4. HETTERSCHEID, W., 'Base circuit design for high-voltage switching transistors in power converters', Technical Note 6, TP1472, Mullard Limited, 1974.

Figs.6 to 9 are on pages 286 and 287

COMPONENT LIST

Resistors

All CR25 5% unless otherwise stated.

R_1	39Ω, CR37 5%
R_2	1kΩ
R_3	1.5MΩ, CR25 10%
R_4	220kΩ, CR37 5%
R_5	1kΩ
R_6	1kΩ
R_7	39kΩ
R_8	10kΩ (adjust on test)
R_9	150Ω
R_{10}	82kΩ
R_{11}	4.7kΩ
R_{12}	390kΩ
R_{13}	2.7kΩ
R_{14}	10kΩ
R_{15}	4.7kΩ
R_{16}	1kΩ
R_{17}	4.7kΩ
R_{18}	330Ω, CR37 5%
R_{19}	12kΩ
R_{20}	470kΩ, CR37 5%
R_{21}	470kΩ, CR37 5%
R_{22}	100Ω
R_{23}	1.8Ω
R_{24}	1kΩ, PR52 5%
R_{25}	100Ω
R_{26}	5.6kΩ, CR37 5%
R_{27}	1kΩ, PR52 5%
R_{28}	1kΩ, PR52 5%

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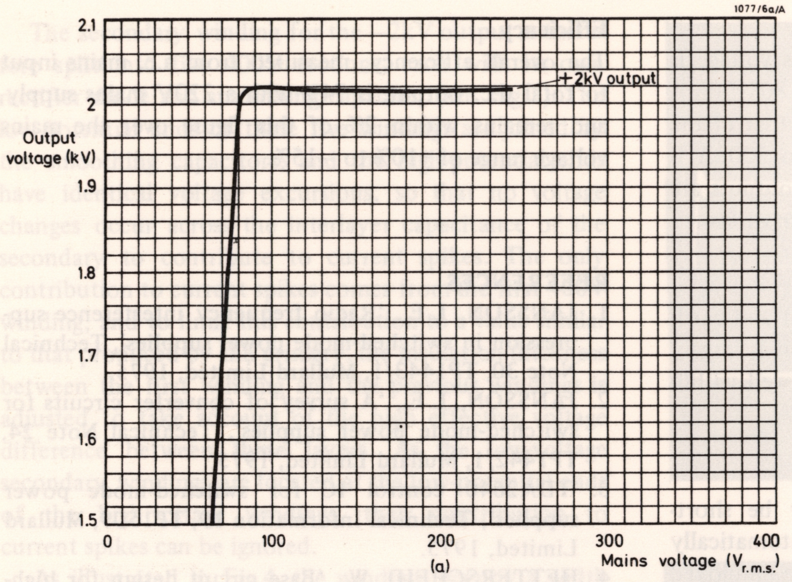
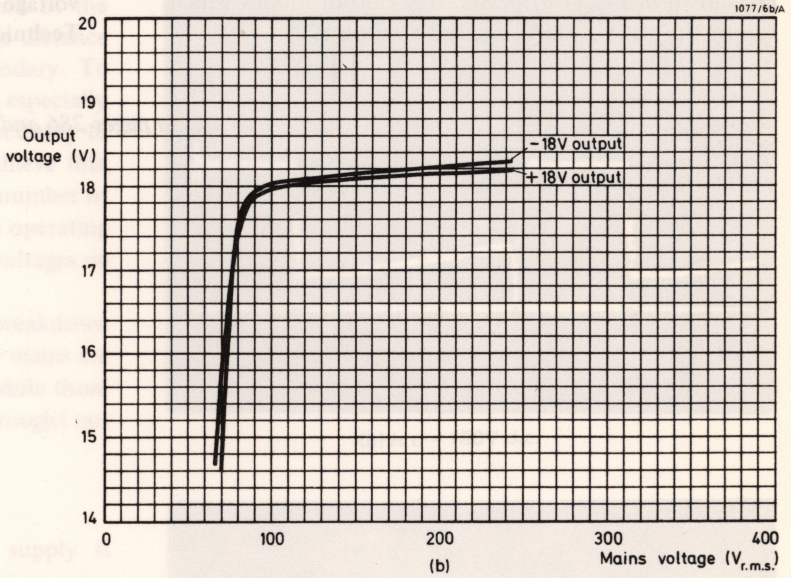




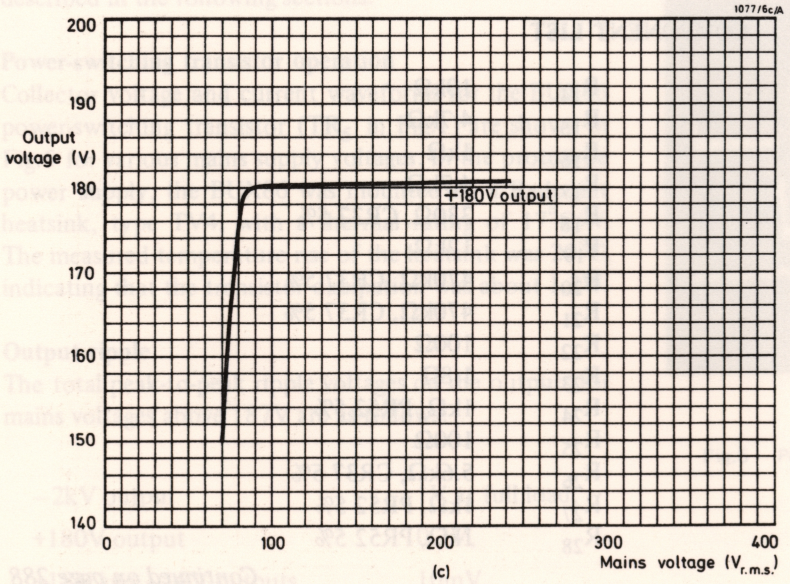


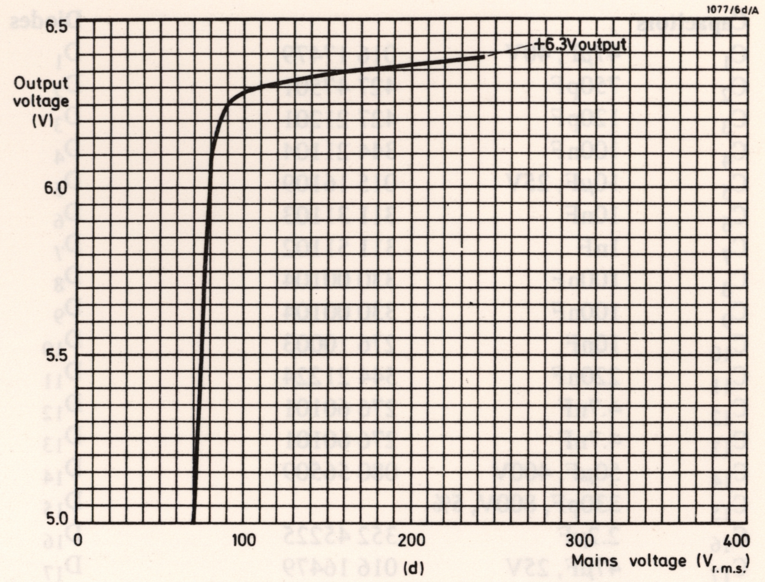
Fig.6 – Output voltage plotted against mains voltage

◁ (a) +2kV output

◁ (b) + 18V, −18V outputs

◁ (c) +180V output

(d) +6.3V output ▷



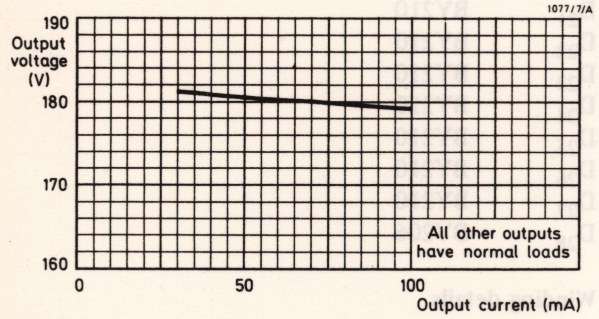


Fig.7 – Output voltage plotted against output current for +180V output

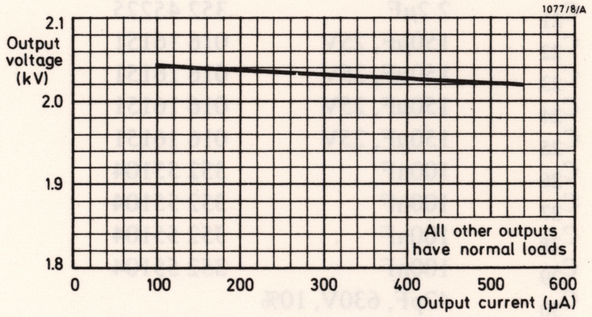


Fig.8 – Output voltage plotted against output current for −2kV output

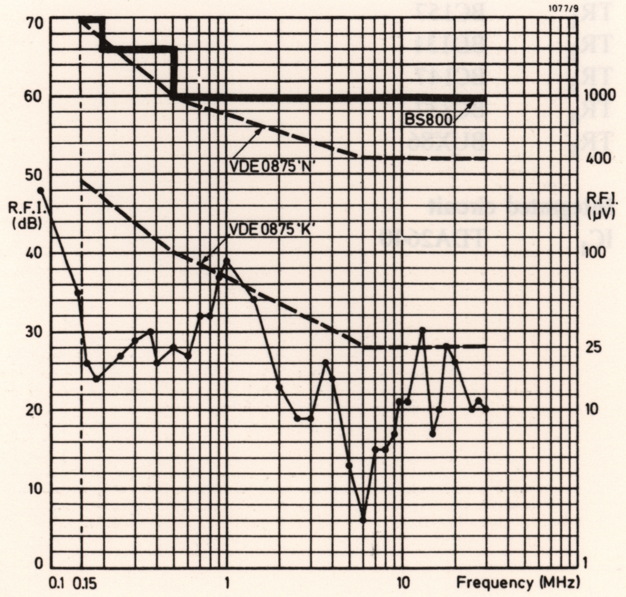


Fig.9 – Radio frequency interference

Capacitors

C_1	47μF, 40V	016 17479
C_2	750pF	427 47501
C_3	120pF	427 21201
C_4	100nF	344 21104
C_5	10μF, 25V	015 16109
C_6	10nF	311 31103
C_7	1nF	311 51102
C_8	100nF	330 00104
C_9	100nF	330 00104
C_{10}	10nF	276 10003
C_{11}	220nF	344 21224
C_{12}	4.7nF	276 60101
C_{13}	4.7nF	276 60101
C_{14}	50μF, 400V	080 56509
C_{15}	330pF, 800V, 5%	
C_{16}	2.2μF	352 45225
C_{17}	47μF, 25V	016 16479
C_{18}	2.2μF	352 45225
C_{19}	2.2μF	352 45225
C_{20}	2.2μF	352 45225
C_{21}	2.2μF	352 45225
C_{22}	150μF, 25V	016 16151
C_{23}	150μF, 25V	016 16151
C_{24}	150μF, 25V	016 16151
C_{25}	150μF, 25V	016 16151
C_{26}	100nF	352 55104
C_{27}	100nF	352 55104
C_{28}	100nF	352 55104
C_{29}	100nF	352 55104
C_{30}	47pF, 630V, 10%	
C_{31}	100nF	352 55104
C_{32}	150μF, 25V	016 16151

Transistors

TR_1	BC157
TR_2	BD131
TR_3	BC147
TR_4	BC337
TR_5	BUX86

Integrated circuit

IC_1	TDA2640

Diodes

D_1	BAW62
D_2	BYX36
D_3	BZY88-C33
D_4	BZY88-C12
D_5	BZY88-C27
D_6	BZY88-C6V2
D_7	BAW62
D_8	BY210
D_9	BY210
D_{10}	BY210
D_{11}	BAW62
D_{12}	BAW62
D_{13}	BY224
D_{14}	BY210
D_{15}	BY210
D_{16}	BAW62
D_{17}	BAW62
D_{18}	BAW62
D_{19}	BY210
D_{20}	BY210
D_{21}	BY210
D_{22}	BY210
D_{23}	BY210
D_{24}	BY210
D_{25}	BY210
D_{26}	BY210
D_{27}	BY210
D_{28}	BY206

Winding details

L_1	100 + 100 turns, bifilar wound, 0.315mm enamelled copper wire, DT2480 former, one pair FX3440 RM8 cores.
L_2	200 turns, 0.315mm enamelled copper wire, DT2480 former, one only FX3440 RM8 core.
L_3	5 turns, 0.315mm enamelled copper wire, FX2249 core.
L_4	2 turns, 0.315mm enamelled copper wire, FX2249 core.
L_5	2 turns, 0.315mm enamelled copper wire, FX2249 core.
T_1	Winding details shown in Fig.4.